

# Nano-lithography for Integrated Circuits - Challenges for Continued Scaling

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## Abstract

*The scaling of integrated circuitry has been afforded by continuous innovation in the field of lithography, the technology by which sub-micron features are patterned on silicon wafers. While numerous lithographic applications have been developed over years, the principle workhorse technology remains projection optical lithography. This process, which involves accurately projecting an arbitrary desired circuit pattern as an aerial image of deep ultraviolet radiation onto a photosensitive material and the subsequent conversion of this projected image of deposited energy into three-dimensional features, has enabled patterning of individual transistors on the order of tens of nanometers with precise dimensional control. As the semiconductor industry drives to ever smaller circuitry, lithographers are increasingly challenged to extend this technology to higher resolution. This presentation addresses the current state of affairs in lithography,*

*highlighting how advances in both optics and materials have led us to where we are today, demonstrating how immersion lithography has allowed for further extension of optical lithography for current technology generations and projecting what the future might look like for continued scaling of integrated circuits.*

## Author Biography

*David Medeiros is the manager of the Advanced Lithography Research team at IBM. His background is in photoresist development for optical and e-beam lithography and other materials development for applications in semiconductor manufacturing. He received his PhD in organic chemistry from the University of Texas at Austin in 1998 and has been with IBM since. He has co-authored numerous papers on photoresist technology and was recently named a Research Master Inventor for his contributions to IBM's patent portfolio. He lives in Yorktown, NY with his wife, son and two dogs.*