An Over 200 dB Dynamic Range Image Capture using a CMOS Image Sensor with Lateral Overflow Integration Capacitor and Current Readout Circuit in a Pixel

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Abstract

An image capturing solution extending dynamic range (DR) over 200 dB has been demonstrated by 64 × 64 pixels 20 μm pixel pitch CMOS image sensor with the lateral overflow integration capacitor and the current readout circuit in each pixel. The operation combining the four times of the voltage readouts and the one time of the current readout has achieved a high S/N ratio performance in the incident light ranging from about 10^{-2} to 10^{8} lx.

Introduction

A DR enhancement is strongly required in addition to a high sensitivity, a high S/N ratio and a high resolution in order to realize the ultimate performance of the image-sensing device for the digital camera, the security, the automotive and the medical applications. Several recent papers have reported the various approaches to extend DR; such as, the multiple exposures in a frame [1-6], the logarithmic compression [7-16], the dual photodiode in a pixel [17], the lateral overflow integration capacitor [18-20] and the combination of the linear and the logarithmic responses [21-24]. These approaches have improved DRs, however still remain in 100 to 140 dB of DRs. In order to extend DR furthermore, the CMOS image sensor featuring the lateral overflow integration capacitor and the current readout circuit in each pixel has been previously demonstrated [25]. This paper describes the over 200 dB DR image capturing method combining the four times of the voltage readout operations and the one time of the current readout operation to keep a high S/N ratio in the incident light ranging from about 10^{-2} to 10^{8} lx.

Device structure and circuit diagram

Fig. 1 shows a schematic diagram of a pixel and a column circuit [25]. The pixel circuit consists of a fully depleted photodiode (PD), a transfer switch (T), a floating diffusion to convert the charge to the voltage (FD), a reset switch (R), a source follower amplifier (SF), a row select switch (X), an overflow photoelectron integration capacitor (CS), a connection switch between FD and CS (S), another transfer switch (T'), current mirror circuits amplifying the photocurrent from PD (CM1, CM2), a reference current source (I_{REF}) and another row select switch (X1'). The column line component consists of a current source driven by the voltage readout operation (I_{vol}) and a current readout circuit of the current readout operation, which includes current mirror circuits comprising CM3 and CM4, a common-gate transistor (X2') and a logarithmic compression circuit (LOG), in each column. The voltage readout circuit with a lateral overflow integration capacitor in a pixel is as same as described in the previous paper [20] and leads to the extension of the DR keeping a high sensitivity and a high S/N ratio without losing the overflow charges from PD. The current readout circuit achieves further extension of the DR to the bright side by reading out the logarithmic compression voltage of the photocurrent amplified in each pixel and column.

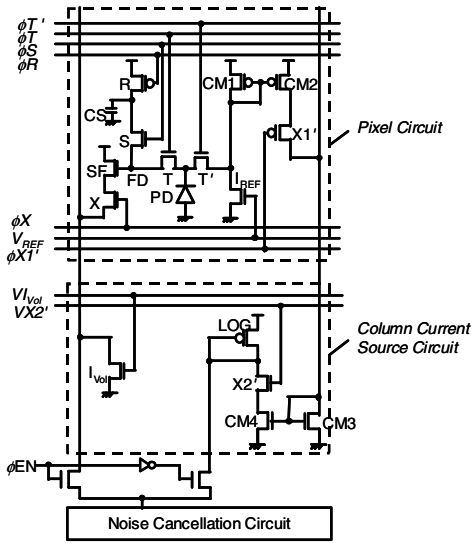

***Figure 1**. Schematic diagram of a pixel and a column circuit [25].*

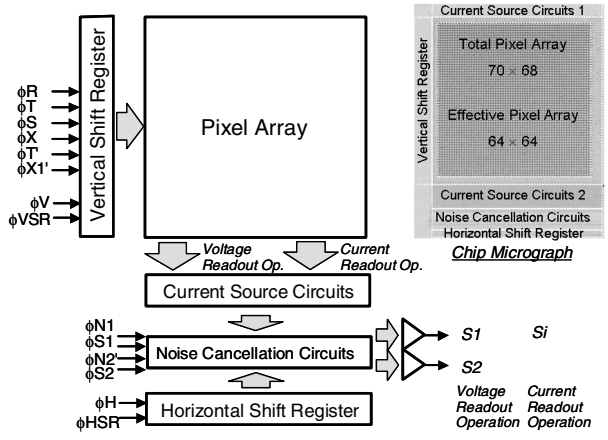

***Figure 2**. Block diagram and chip micrograph [25]. The chip size is 2.6 x 2.6 mm^2.*

Fig. 2 shows the image sensor block diagram and the chip micrograph [25]. The image sensor with 64(H) × 64(V) pixels in the effective image area and a 20 × 20 m^2 pixel size is fabricated through a 0.35 m 2P3M CMOS technology.

Image capturing method and results

Fig. 3 shows the timing diagram of the pixel circuits. The voltage readout operations follow the same timing diagram as described in the previous paper [20, 25] and, in addition, incorporates the electrical shutter operation. During the integration period (t_3), the signal charges are integrated by PD until it reaches saturation, then the overflow charges are integrated at FD + CS via the switches T and S. This operation enables the overflow charges from PD to be utilized for the signal. After the integration (t_4), the charges distributed to FD are readout as the noise N1 by turning the switch S off. The signal charges are transferred from PD to FD by turning the switch T on (t_5) and readout as the signal S1 + N1. The signal charges at PD are fully transferred to FD + CS by turning the switch S on (t_6) and then readout as the signal S2 + N2. The high tolerance of the signal S2 for the dark current shot noise and the reset noise is achieved by the mixture of the signal charges. FD + CS is reset by turning the switches T and R on (t_1') and the reset noise N2' is readout by turning the switches R and T off (t_2'). The noise N2' includes the fixed-pattern noise caused by the variation of the threshold voltage of SF. In the shortest exposure of 1/130ks, the signals of N1, S1, S2 and N2' are readout by keeping the switch T on and achieving a high charge transferring efficiency from PD to FD. In the voltage readout operations, the signals N1, S1 + N1, N2' and S2 + N2 are readout from each pixel. The noise subtractions (S1 + N1) - N1 and (S2 + N2) - N2' are performed by the on-chip noise cancellation circuit. Either the noise-subtracted signal S1 or S2 is selected by the pixel as compared with the reference voltage level.

The current readout operation consists of two phases, one is the reference-current readout and the other is the reference-current plus signal-current readout. The reference-current readout is performed by turning the switches R, S, T, and X1' on, and T' and X off (t_{1i}), applying V_{REF} to the gate of the transistor that produces I_{REF}, and keeping the reference current. The reference current is amplified by the pixel- and column-current mirror circuits and finally converted to the logarithmic compressed reference voltage Ni. Then the photocurrent at the PD and the reference current are readout from the same path by turning the switches R and T off and the switch T' on (t_{2i}), and the signal voltage superimposed on the reference voltage Si + Ni is obtained. After that, the signal Si is readout by subtracting the Ni from the Si + Ni through the on-chip noise cancellation circuit. Even in the current readout operation, the variation of the amplification factor by pixel and column is cancelled by this method.

The 200 dB DR image capture is performed by the sequentially combining the voltage readout operations with the varied exposure time controlled rolling electric shutter and the current readout operation. The voltage readout operation achieves an over 100 dB DR by one time exposure. The four times of the exposures with varied time extend DR up to 160 dB in the incident light ranging from 10^{-2} to 10^6 lx. Furthermore, the image capture in the extremely bright light ranging from 10^6 to 10^8 lx is performed by the current readout operation.

Fig. 4 shows the signal switching methods. Taking one of the voltage readout operations as an example shown in Fig. 4(a), the non-saturated signal S1 is compared with the reference voltage V_{REF1}. Either the non-saturated signal S1 or the over-saturated signal S2 is selected when S1 is lower or higher than V_{REF1}. The V_{REF1} is normally set a bit lower than the saturation voltage of the non-saturated signal S1 so that the variation of the saturation voltage does not affect the performance. It is also set to achieve the S/N ratio in S2 over 40 dB at the signal switching point. The

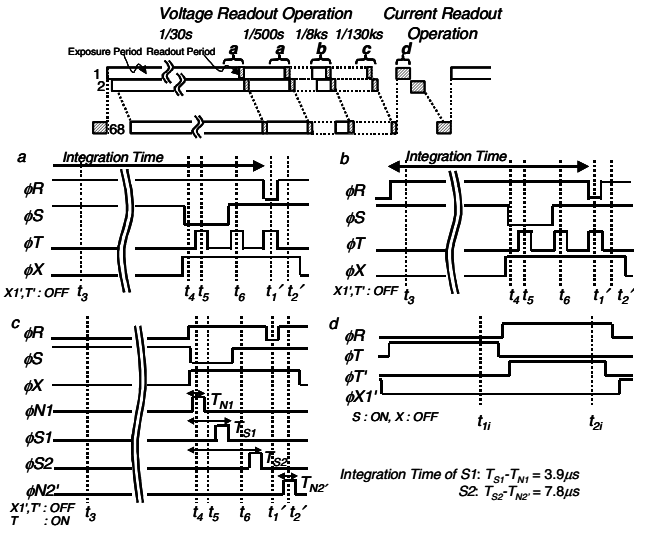

***Figure 3**. Timing diagram.*

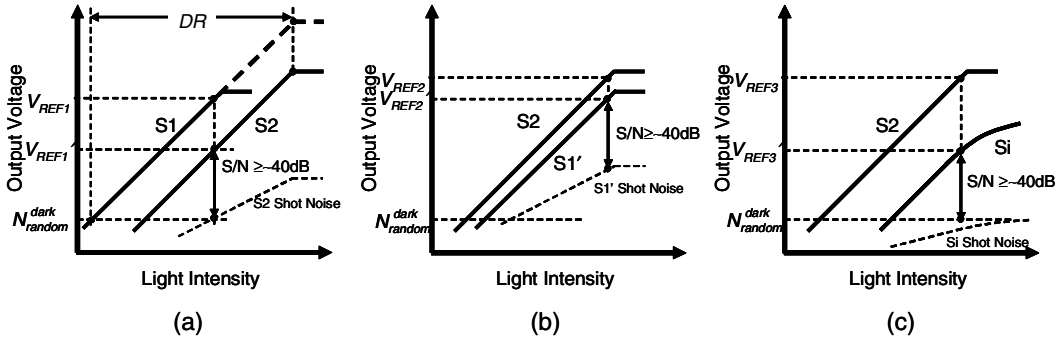

***Figure 4**. Signal switching methods (a) in one voltage readout operation. (b) in two successive voltage readout operations. (c) between voltage readout operation and current readout operation.*

over 100 dB DR signal keeping a high S/N ratio is obtained.

In the two successive readout operations shown in Fig. 4(b), the over-saturated signal S2 of the previous voltage readout operation is compared with the reference voltage V_{REF2}. Either the signal S2 or the non-saturated signal S1' of the next voltage operation is selected according to the lower or the higher S2 than V_{REF2}. The V_{REF2} is set a bit lower than the saturation voltage of S2 to achieve the S/N ratio of S1' over 40 dB at the signal switching point.

In the shortest exposure readout operations and the current readout operation shown in Fig. 4(c), the over-saturated signal S2 of the shortest exposure voltage readout operation is compared with the reference voltage V_{REF3}. Either the signal S2 or the current readout operation signal Si is selected when S2 is lower or higher than V_{REF3}. The V_{REF3} is set a bit lower than the saturation voltage of S2 to achieve the S/N ratio of Si over 40 dB at the signal switching point.

Fig. 5 shows the photoelectric conversion characteristics on the two vertical scales of the input-converted voltage for all the signals, and the digital signals [25]. In the voltage readout operation, the rolling electrical shutter time is sequentially varied as 1/30s, 1/500s, 1/8ks and 1/130ks, shortening the exposure time by about 1/16 between the respective steps. The voltage readout operation with four splits of the exposure time shows linear responses in the incident light ranging from about 10^{-2} to 10^{6} lx and extends the DR up to about 160 dB. In addition, the current readout operation also realizes good photoelectric conversion characteristics from about 10^{5} to 10^{8} lx. The hybrid operation of the voltage and the current readouts is found to extend the DR over 200 dB.

Fig. 6 shows the S/N ratio characteristics in the incident light ranging from about 10^{-2} to 10^{8} lx. The solid line and square points are the calculated and the experiment data respectively. In the voltage readout operations, the S/N ratio around 10^{-1} lx or less is contributed by the dark random noise still remaining after the noise reduction operation of (S1 + N1) - N1. The S/N ratio around 10^{-1} lx or more is contributed by the photon shot noises. In the current readout operation, the noise originates in the signal processing circuits in the outside of the sensor chip and the S/N ratio will improve if the noise is decreased. It is found that the calculated values and the experimental values indicate a good agreement and the S/N ratio is about 40 dB at all switching points.

Fig. 7 shows the sample images synthesized to over 200 dB DR (about 34 bit length). In each image, 8 bit data is displayed with 2 or 4 bit shift from the lower digit to the upper digit and the lens iris fixed at F-number of 1.4. It is found that the image sensor is capable of capturing various scenes with the incident light ranging from about 10^{-2} to 10^{8} lx with high quality images.

Conclusion

A high S/N ratio image capturing method of the over 200 dB DR CMOS image sensor with lateral overflow integration capacitor and current readout circuit in each pixel is demonstrated. This technology is extendable to the various applications requiring the high sensitivity, high S/N ratio and hyper wide DR performance.

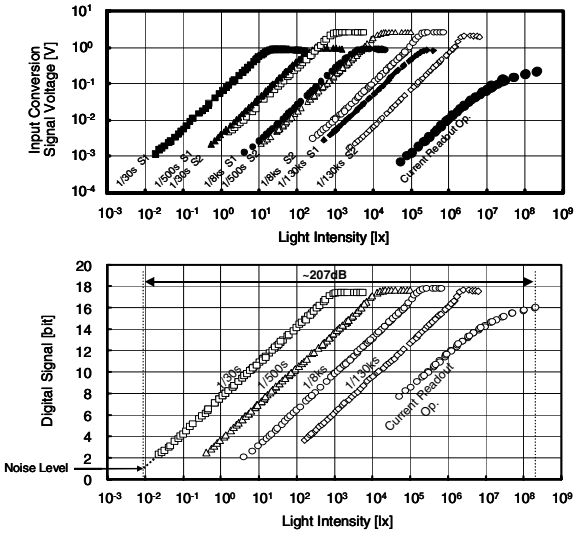

Figure 5. *Photoelectric conversion characteristics [25].*

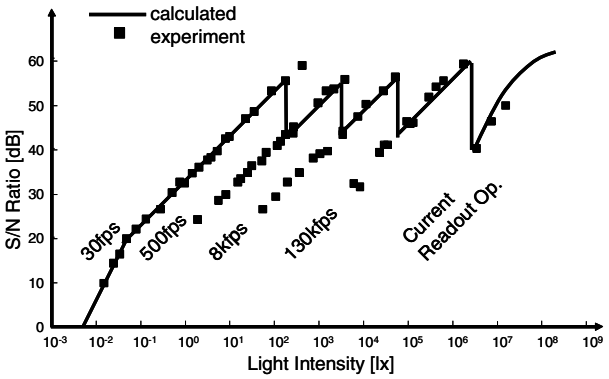

Figure 6. *S/N ratio characteristics.*

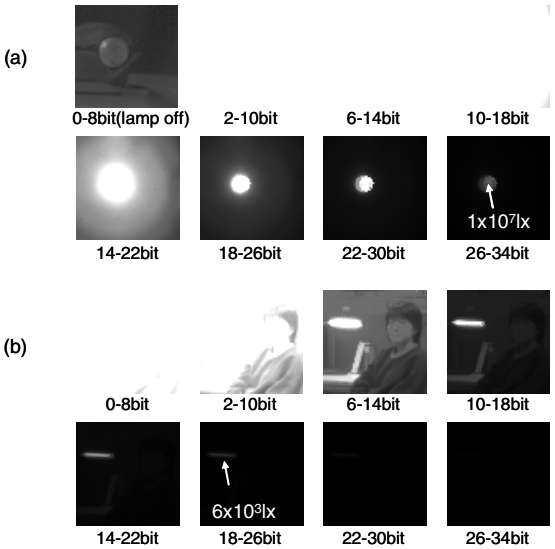

Figure 7. *Sample images. (a) A high luminance Metal halide lamp (b) A lady by a florescent light*

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