Dark Current Reduction Techniques for Wide Dynamic Range Logarithmic CMOS Pixels

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Abstract

CMOS logarithmic pixels are capable of simultaneously imaging more than 6 decades of light intensity. However, their low light sensitivity is limited by the inherent leakage current of a CMOS process that flows through the load transistor in the pixel in parallel with the photocurrent. In this paper, we will discuss various approaches based on process, circuits and layouts to reduce this dark current. Results from two different approaches will then be reported. The first approach uses a novel circuit to maintain the voltage around the photodiode as close to zero as possible. The second approach uses a new layout for the logarithmic pixel to reduce the dark current arising from the edges of the photodiode.

Introduction

CMOS based logarithmic pixels such as the one shown in figure 1, are capable of imaging more than 6 decades of illumination by logarithmically compressing the photocurrent generated by the diode *PD* using the subthreshold transistor $M1$. Transistors, $M2$ and $M3$, act as a source follower-switch combination and form the first part of the signal readout circuitry. The dynamic range of such pixels is significantly higher than that of both CCDs and CMOS- based active pixel sensors [1]. Other advantages of these pixels include a small output voltage range, which is ideally suited to the reduced voltage range of future deep sub-micron processes, and that a fewer number of bits is required to represent wide dynamic range scenes.

Ideally, the current flowing through the source of transistor, $M1$, is the photocurrent generated in the photodiode. However, previous results have shown that there is an additional contribution to the current flowing through the load transistor [1]. This additional contribution, which flows in the absence of light is known as the dark current, and arises from leakage currents in the pixel. In this paper we study the effects of high dark current in a logarithmic pixel and report the results of some dark current reduction techniques. In the next section, the importance of a low dark current for logarithmic pixels shall be described. There are three different approaches to reduce the dark current. The ideal but expensive approach to reduce dark currents is process modification. However, some circuit and layout techniques hold the promise of reducing the dark current, even in an unmodified process. A circuit modification and a layout based technique to reduce dark current are investigated in this paper. Test results from structures manufactured in an unmodified 0.35μm process are presented for both techniques.

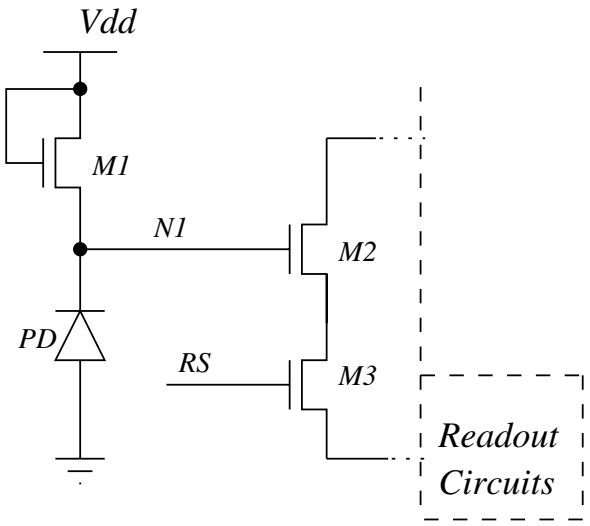

Figure 1. *A typical logarithmic Pixel*

Low Dark Current

The response of a logarithmic pixel to a photocurrent x in the presence of a dark current c can be modelled as [1]

$$y = a + b\log(x + c) \tag{1}$$

where a represents an offset voltage and b is the pixel gain. From this model, it is immediately apparent that the pixel will only respond to changes in photocurrent when $x > c$, as shown in Figure . Less obviously, the dark current has an adverse effect on the procedure that is required to compensate for the variations between responses of individual pixels that give rise to fixed pattern noise. In particular, it has been observed in previous work that fixed pattern noise correction, as shown in Figure , is only effective for photocurrents that are more than two orders of magnitude larger than the dark current [2]. The dark current therefore has a severe effect on limiting the lowest illumination condition in which a logarithmic pixel can operate successfully. Any reduction in dark current of a logarithmic detector will hence improve the performance of the pixel dramatically.

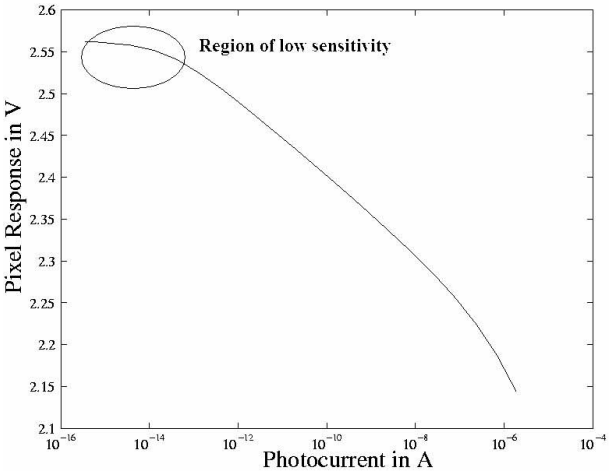

Figure 2. *Figures showing Loss of sensitivity at low photocurrents due to high dark current in the response of logarithmic pixels*

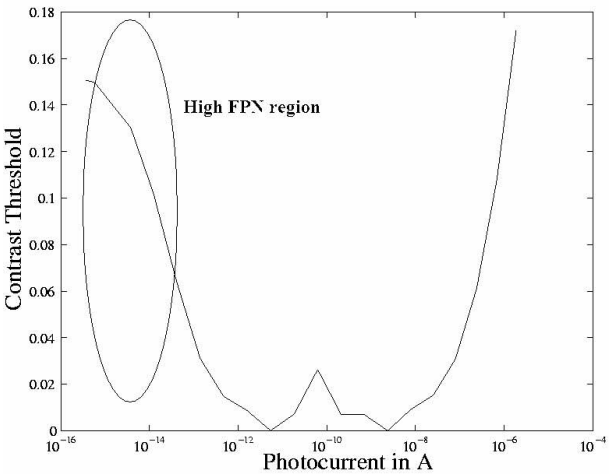

Figure 3. *The residual fixed pattern noise after correction for offset and gain variations over a range of photocurrents showing the degradation in performance at low photocurrents.*

A photodiode in a typical CMOS process has a leakage current of the order of $1nA/cm^2$ [4]. It is possible to modify a typical CMOS manufacturing process to enhance the photosensivity of the pixel and/or reduce the leakage current. Several fabrication companies, including TSMC, Tower Semiconductors, DongbuAnam semiconductor, and IBM have reported processes which have included special step to fabricate the low dark current photodiodes. However, these process modifications add to the cost of the manufacturing process and therefore the cost of the final product.

Circuit Technique

Some circuit techniques also improve the performance of pixels at low light. In one of these, the current gain in the pixel is boosted, depending on the region of operation. For example Ward and coworkers have proposed a circuit of two bipolar transistors, wherein, both transistors are used to provide gain at low light levels, by forming a Darlington pair with a high current gain [5]. At medium light levels, only one transistor is used to obtain gain and neither is used at high levels. This circuit enhances the signal value. However, it does not reduce the leakage current.

In order to reduce the leakage current, a circuit modification to reduce dark currents in the photodiode has been investigated. This technique is based upon the fact that the dark current in a photodiode is the reverse saturation current flowing through a reverse biased diode. An interesting feature to note in the I-V characteristic of the diode is the transition between the forward (high positive current) to reverse biased regions (low negative current). At zero voltage across the diode, the reverse saturation current is zero, and hence the current flowing through the diode consists of the photocurrent only. Hence a pixel, which is able to maintain a zero potential across the photodiode, should have minimal leakage current. A circuit to reduce the reverse bias voltage across the photodiode that has been investigated is the double current mirror structure, shown in Figure 4. In this circuit, transistors, $M0$ and

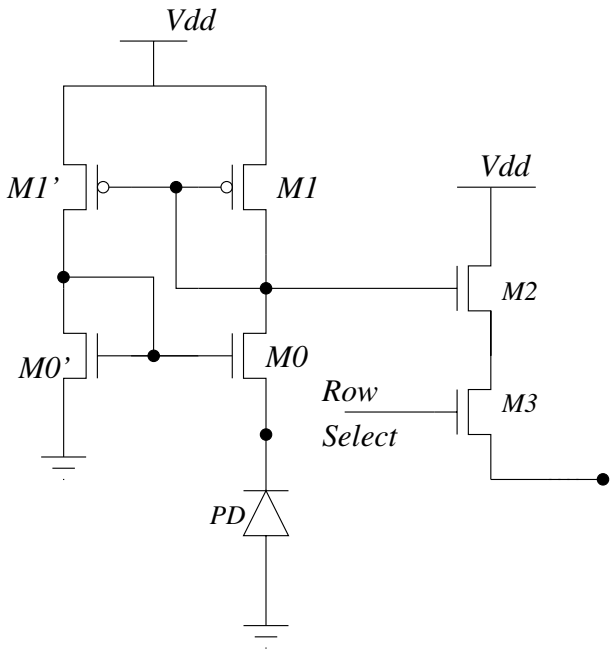

Figure 4. *A double current mirror(DCM) pixel*

$M0'$ form an nMOS current mirror and $M1$ and $M1'$ form a pMOS current mirror. The transistors $M2$ and $M3$ form the first stage of differential amplifier readout circuits [2]. For the currents in the two sides of the circuit to be equal, as required by the pMOS mirror, the gate-source voltage of the two nMOS transistors should be equal. This in turn means that the voltage at the source of $M0$ should be zero. This voltage, being the reverse biased voltage of the photodiode, will ensure that the leakage current of the photodiode remains zero for all photocurrents.

A 100×10 array of these pixels, having dimensions of $10\mu\text{m}\times10\mu\text{m}$, with a differential amplifier readout as used by Choubey and coworkers [2], was manufactured in a typical 0.35μ CMOS process from Austrian Microsystems (CSI).

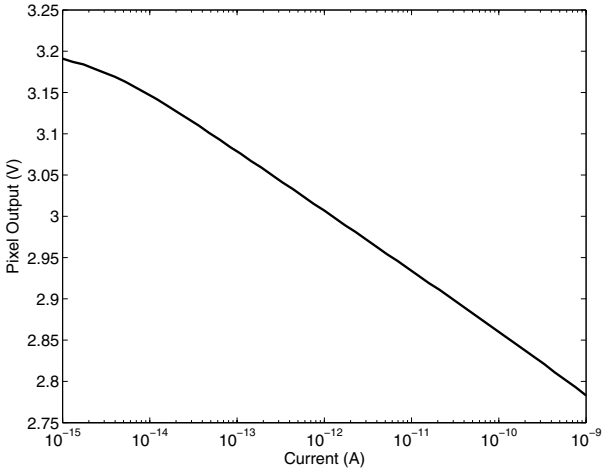

Figure 5. *Pixel Output vs Photocurrent for the DCM pixel*

Parameter of the	Pixel	DCM Pixel	Conventional Pixel
Offset	Mean	1.79	1.74
(V)	SD	0.056	0.017
Gain	Mean	94.0	66.8
mV/decade	SD	4.40	1.01
Bias	Mean	3.64	2.61
(fA)	SD	1.29	0.63

Extracted parameters and their Variation for double current mirror and conventional Pixel

To study the leakage current of these pixels the three parameters of the pixel model, i.e. equation 1, were extracted. The data used for parameter extraction was obtained by exposing the pixel array to uniform scenes of different light intensities generated using a uniform light source and neutral density filters. The parameters and the photocurrent at these intensities were calculated by methods described in the appendix. As shown in Figure 5, the pixel showed a logarithmic response. In order to compare this response with that of a conventional pixel, results were also obtained for a conventional pixel with a similar readout circuit manufactured on the same substrate.

It was observed that the gain in the DCM pixels, of 94mV/decade, is significantly higher than the conventional pixels, which ia approximately 67 mV/decade. It is an expected result because the DCM uses a pMOS load transistor which provides a higher gain. Again as expected the mean offset values in the two types of pixels are comparable because both the pixels have similar readout circuitry. The variation of the offset in DCM pixel was found to be higher than that of conventional pixel. This can be attributed to use of pMOS transistors that are more variable than nMOS transistors for this particular process. The leakage dependant bias parameter unfortunately is larger and more variable for the DCM pixel.

Contrary to our expectation the DCM pixel has a larger dark current than the conventional pixel. It appears that the double current mirror pixel is failing to maintain a small enough bias across the photodiode to reduce its leakage current. This may be because the DCM pixel essentially depended upon the correct operation of the two current mirrors. To minimise the pixel area only small devices can be used in the current mirror and it appears that the resulting mismatch between devices may mean that the circuit is too far from ideal to be useful.

Layout Techniques

Failure of the circuit techniques prompted an inquiry into the potential to use circuit layout to reduce the diode leakage currents. One of the principal components of dark current is the edge leakage currents. These currents owe their origin to the defects at the n^+-diffusion field oxide interface caused by mechanical stress effects and/or contamination. Kopley, Vook and Dungan have proposed a biased guard layer, preferably of a conductive material, to block the doping of the active area diode during fabrication in an active pixel sensor [3]. If the guard layer is biased below the threshold voltage for formation of a channel, this structure reduces leakage currents by separating the photodiode from the field oxide. Cheng and King have used a similar structure, but have utilised a n+ reset ring structure to reduce the dark current in active pixel sensor [4].

In order to test the possibility of reducing leakage current using such a guard ring, simple logarithmic pixels, as shown in figure 1, were manufactured with and without guard rings. Figure 6 shows the layout of a 10μm$\times 10\mu$m simple logarithmic pixel, with a guard ring designed to be manufactured on an 0.35μm process with a fill factor of 40%. Similarly, figure 7 shows the same pixel without the guard ring structure. In the layout with the guard ring, the photodiode has been encircled by the thinnest possible ring of polysilicon, to separate the diffusion and field oxide region. This guard ring needs to be biased at a voltage below the threshold voltage of the technology. In an active pixel sensor, this guard ring can be used as the reset gate of the pixel to reduce its impact on the fill factor. However, in a logarithmic pixel this reset transistor is replaced by the load transistor which operates in subthreshold. To accommodate this transistor, the photodiode is connected to the load device using a metal bridge across the guard ring which is provided with a separate bias connection. In addition, our previous experience of electronic calibration of pixels in this technology has shown that the device leakage currents through nMOS devices with a zero gate-source bias are comparable to the dark current of the photodiodes used. This leakage current however reduces to insignificant values when a negative gate-source voltage in excess of -250mV is used. In this layout the guard ring around the photodiode therefore acts as the gate of an nMOS transistor in which the photodiode acts as the drain and the surrounding region acts as the source. Applying a positive voltage to the bias for the source and a zero voltage to the guard ring will ensure a negative gate-source bias on this guard transistor. Comparison of the figures 6 and 7 shows that by placing the connection for the source bias of the guard nMOS over the non-photosensitive region of the adjacent pixel, it is possible to accommodate the guard structure with a minimum reduction in fillfactor. To allow a comparison of the effectiveness of the guard structure a small array of $100\times$ 10 pixels of both the kinds have been fabricated on a typical 0.35μm CMOS process from Aus-

tria Microsystems (C35). However, due to a change of the typical 0.35μm CMOS process offered by the foundry, we were not able to manufacture this chip on the earlier process.

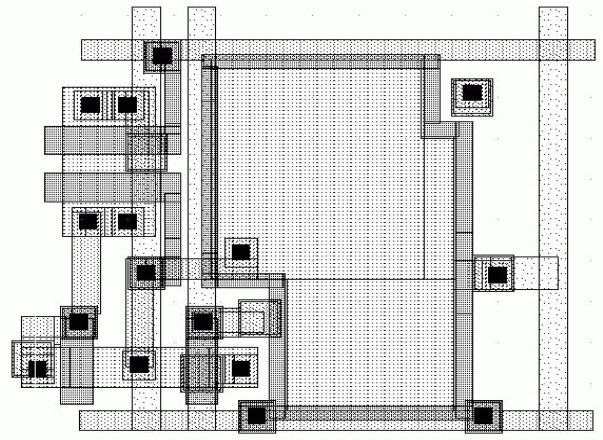

Figure 6. *Layouts of the logarithmic pixels with the guard ring, to reduce the leakage current.*

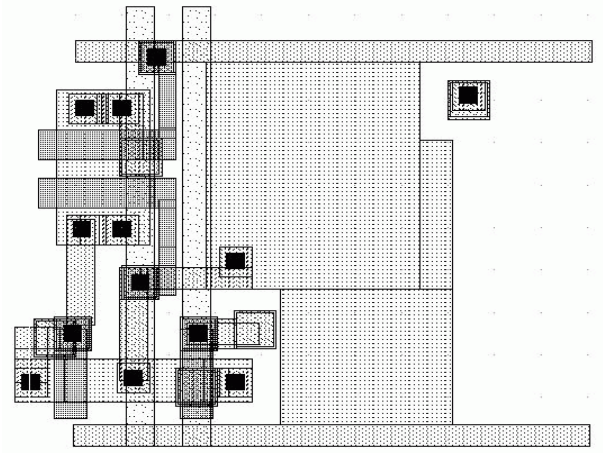

Figure 7. *Layouts of the logarithmic pixels without the guard ring.*

Experiments involving these chips were conducted with electronically generated uniform scenes. The three parameters of the two arrays of pixels are summarised in the following table.

As expected the offset and gain parameters of the two different pixels are very similar. It may be noticed that these values are lower than the last chip due to use of a source follower readout circuits in place of a differential readout circuit. It can also be seen that the mean value of the dark current related parameter of the layout with the guard ring is approximately half of that of the pixel without the guard ring. The dark current of both the pixels is less than the earlier pixels, possibly due to a change in the process used. In addition, the variation of the dark current related parameter has also been reduced to one third of its original value. This means that the worst case dark current in the pixel array is expected to be reduced by a factor of between two and three by using the guard ring. In fact our results showed that in addition to

Parameters of the	pixel	Without guard ring	With guard ring
Offset (in mV)	Mean	680	668
	Std	8.9	9.2
Gain (in mV/decade)	Mean	55.8	56.2
	Std	0.26	0.28
Bias (in fA)	Mean	0.75	0.31
	Std	0.37	0.10

Extracted parameters and their variations for the pixels with and without guard ring

reducing the mean and the standard deviation of the dark current related parameter, the presence of the guard ring also eliminated some particularly high dark currents, that occurred near the edge of the array of pixels without a guard ring. Using the guard ring therefore reduced the worst case dark current from 2.8fA to less then 0.6fA. The worst case dark current is therefore reduced by a factor of almost five.

Conclusion

Dark currents limit the function of logarithmic pixels. It not only affects the lowest measurable illumination, it also decreases the sensitivity of a logarithmic pixel at low light levels. Further it also reduces the usefulness of offset and gain calibration schemes. Three approaches of reducing dark current have been described in the paper. Of these, process modification is ideal but costly. A circuit based scheme using a double current mirror to maintain the voltage around the photodiode close to zero has been investigated with disappointing results. Dark currents, can however, be reduced by using a protective guard ring of conductive material. Proper biasing of this structure further reduces the dark operation in pixel operation.

Appendix: Parameter Extraction Strategy

The strategy that has been used to determine the photocurrent and the effective dark current in each pixel in the array is based upon the technique that has been used previously to determine the offset and gain variations between logarithmic pixels [2]. This technique is based upon the three parameter model of the pixel response of equation 1 The offset and gain parameters of each pixel can be calculated using the pixel responses, y_1 and y_2, at two photocurrents, x_1 and x_2, significantly higher than the dark current. In particular, this means that the lower of these two photocurrents should be approximately one hundred times larger than the maximum expected dark current. This reduces the effect of the dark current on the pixel response to less than 1%. The second photocurrent then has to be significantly larger than the first photocurrent to reduce the effects of temporal and quantisation noise on the calculation of the gain parameter. However, if this second current is too large then the load transistor will be forced to operate in moderate inversion and the simple three parameter model will no longer be valid, hence the high residual fixed pattern noise at large photocurrents in Figure 2. Experience has shown that the best strategy is to use a photocurrent that is approximately 300 times larger than the first photocurrent. The offset and gain para-

meters can then be extracted using the equations

$$b = \frac{y_1 - y_2}{\log(x_1/x_2)} \quad (2)$$

$$a = y_1 - b\log(x_1) \quad (3)$$

The final step in determining the dark current related parameter is then to use these two parameter values and the response of the pixel in the dark, y_d, using the equation

$$c = \exp\left(\frac{y_d - a}{b}\right) \quad (4)$$

The two photocurrents can be generated by illuminating the array of the pixels with two uniform but different light intensities. However, it is more convenient to generate a bias current for each pixel electronically using a calibration current source present in every column [2].

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Author Biography

Bhaskar Choubey received his B.Tech. from Regional Engineering College(now NIT), Warangal, with a Gold Medal for best outgoing student. He is working in University of Oxford, as a Rhodes Scholar, in the field of wide dynamic range CMOS imagers. In 2005, he was a visiting scientist at Max Planck Institute of Brain Research, on a Scatcherd fellowship, working on psychophysics of human vision.

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Steve Collins received a B.Sc. in Theoretical Physics from the University of York in 1982 and a Ph.D. from the University of Warwick in 1986. From 1985 until 1997 he worked at the Defense Research Agency on various topics including the origins of 1/f noise in MOSFETs, image sensors and analogue information processing. From 1997 he has been at the University of Oxford were he has continued his interest in smart imaging sensors and non-volatile analogue memories.