Imagers for professional digital photography

Jan Bosiers, Bart Dillen, Cees Draijer, Inge Peters; DALSA Professional Imaging; High Tech Campus 12a, 5656AE Eindhoven, The Netherlands

Abstract

We present two new full-frame CCD imagers for professional digital imaging applications: a 33M-pixel imager on 36mm x 48mm format for studio photography, and a 28M-pixel imager on 44mm x 33mm format for social photography. Both imagers use the same newly developed 7.2 x 7.2 μm^2 pixel and the same optimized low-noise, high-speed output amplifier. The 28M-pixel CCD incorporates a new feature in CCD operation: on-chip RGB-compatible charge binning and sub-sampling.

Introduction

The drive for better image quality for the most demanding professional digital imaging applications has resulted in an increase both in resolution and in imager size: from 6M and 11M pixels on 24mm x 36mm format in 1998 and 2001 [1], [2], [3] to 22M pixels on 36mm x 48mm format in 2004 [4]. In this paper, we introduce a 33M-pixel imager on 36mm x 48mm format for studio photography, and a 28M-pixel imager on 44mm x 33mm format for social photography. First the system requirements for imagers used in professional digitals still camera (pro-DSC) applications are presented. The basic architecture and operation of full-frame CCDs for pro-DSC applications will be explained. We will then focus on optimization of the pixel and output amplifier for the new 28M-pixel and 33M-pixel imagers. We will present RGB-compatible charge binning as a unique new feature. The evaluation results for these imagers conclude this paper.

Imagers for professional DSC applications

The imagers for pro-DSC applications are used in professional camera backs and large-format digital single-lens reflex (D-SLR) cameras. The major drives in this application are image quality and resolution. Excellent image quality under all lighting conditions is essential. This implies high sensitivity and low noise, high dynamic range and excellent highlight handling, even with shrinking pixel sizes needed to satisfy the requirements for higher resolution. The compatibility with system lenses determines the optical format and angular response [4], [5]. Finally, high-speed image capture and readout, and unique features are important competitive aspects for pro-DSC applications.

Currently, CMOS imagers as well as full-frame CCDs are used for DSC applications. We will show that frame-transfer CCDs with vertical anti-blooming give the best possible fit with the application requirements.

Full-frame CCD imager with vertical anti-blooming

The full-frame CCD architecture (DALSA True Frame™) was used to build the 33M- and 28M-pixel imagers. The floor plan of the 33M-pixel imager is shown in Fig.1. It consists of an array of 5040 x 6726 four-phase CCD pixels with RGB Bayer color filter pattern and two three-phase readout registers, one at the top and at the bottom of the array. Black reference columns and rows are provided by covering active pixels with a metal light shield. At each corner of the device, an output amplifier is provided. Since both the pixel array and the register have the option of split readout (top-bottom for the pixels, left-right for the register), the user can choose, by means of the pulse pattern, to use one, two or four outputs.

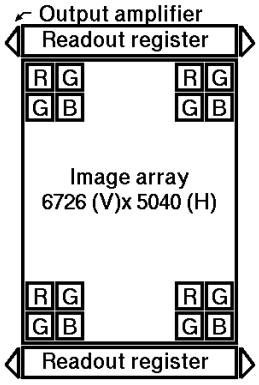

***Figure 1**. Floor plan of 33M-pixel CCD for professional DSC applications*

The n-type buried CCD channel for the pixel array and for the readout register is built in a p-well on an n-type substrate. The resulting vertical npn-structure supports vertical anti-blooming in combination with electronic shutter in the image pixels. The implant profiles were optimized for optical sensitivity, charge capacity, highlight handling, dark current and transport efficiency.

At the start of the exposure, the pixels are emptied of previously collected electrons. Then the mechanical shutter is opened. After closing the shutter, the sensor is read out line per line through the readout register(s).

Design for Image Quality

Fig.2 shows a top view and cross section of the 7.2 x 7.2 μm^2 pixel. A four-phase structure is obtained by using two layers of transparent membrane poly-silicon as gate electrodes [6]. The optical and electrical performance was optimized by a special etching technique that results in a very planar structure with adjacent (i.e. non-overlapping) gates. Vertical metal-1 straps yield sufficiently low RC-times to maintain good transport efficiency also at higher frequencies. The vertical anti-blooming (VAB) structure was preferred above the lateral anti-blooming since VAB does not compromise the fill factor. It guarantees a better and more symmetrical pixel separation and thus a better MTF. In addition, VAB allows a very fast electronic shutter: previously collected electrons do not need to be read out line by line, but the pixels are emptied in less than 10µs simply by setting all the image gates to 0V and by applying a +5V pulse to the substrate.

On top of the image pixels, a narrow metal-3 grid pattern is used to optimize the RGB pixel separation. The resulting optical

fill factor is 70%. This high fill factor implies that no microlenses are needed that could compromise the angular response [5], [7].

The three-phase readout register and the output amplifiers were designed for operation up to 25MHz. The three-stage source follower output amplifier was optimized for low noise, high linearity and high conversion gain.

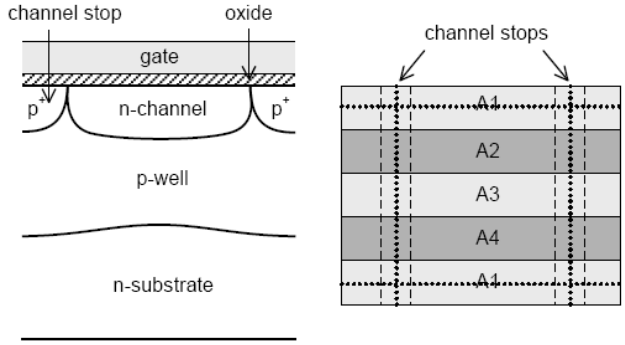

***Figure 2**. Top view and cross-section of 7.2 x 7.2 um² pixel*

High Speed

The increase in resolution of the imager implies longer readout times, thus reducing the maximum frame rate. Increasing the readout frequency above 25MHz poses problems in the application, e.g. the availability of front-end ICs with 14 bit ADC resolution. A better solution is to offer the option of multiple outputs, user-selectable by means of the pulse pattern. For multiple output operation, the vertical straps have a split in the middle of the image section. Similarly, the horizontal register connections have a split in the center.

RGB compatible charge binning

In studio photography, resolution is still the major driver. However, for social photography, some conditions are less demanding with respect to resolution, but require a higher sensitivity, better signal-to-noise ratio, higher frame rate or less storage capacity. To combine these requirements, the 28M-pixel CCD imager was provided with a novel 2 x 2 on-chip RG_rG_bB-compatible charge binning concept (G_r is green pixel in red line, G_b is green pixel in blue line,). With the charge-binning mode turned "on", the resolution is decreased by a factor four, but the sensitivity, the signal-to-noise ratio and the frame rate are increased. The sensitivity is increased by a factor of four. The signal-to-noise ratio is improved two times, when the signal is shot-noise limited and even four times, when the noise in the signal is dominated by the amplifier noise. Also the image file size is reduced by a factor of four. In full resolution mode the binning feature is turned "off", and the sensor is operated as before.

A schematic view of the RGB binning architecture is depicted in Fig.3 [8]. Parallel to the horizontal readout register the novel RGB binning structure, consisting of binning transfer gates (BTG) and storage gates (STG), has been designed. One BTG and one STG are used per two neighboring columns.

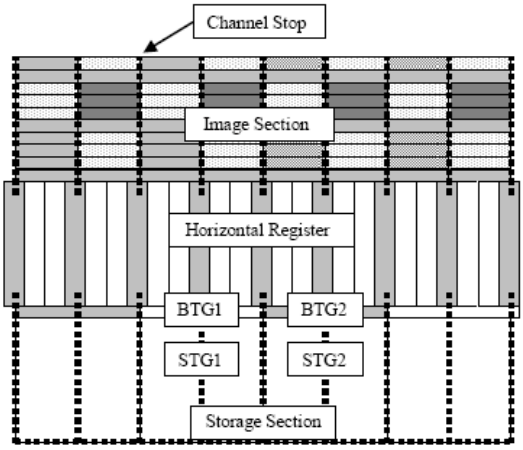

***Figure 3.** Schematic view of RGB binning architecture*

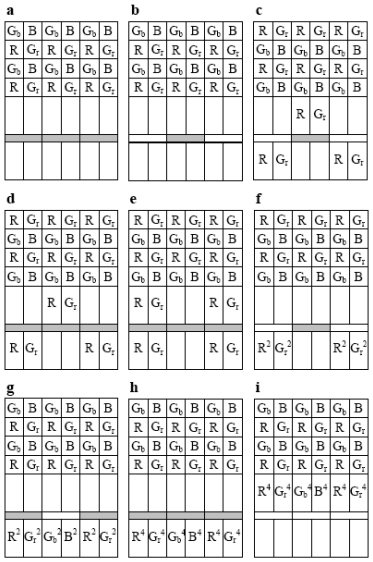

***Figure 4**.RGB binning operation*

The RGB binning operation is explained in Fig.4. In (a) the starting point is depicted; no charge in horizontal register cells and in storage cells. In (b) the BTG cells are alternately opened or closed. In (c) one line of the image section is transferred to the register section. Since the BTG cells are alternately opened and closed some of the charge packets will stay in the horizontal register and others will be transferred to the storage cells. This is done in color pairs (RG_r-pair in this picture), because one BTG and STG is used per two columns. In (d) all BTGs are closed, so that charge packets in horizontal register and storage cells are separated. In (e) two standard horizontal transport cycles have been performed to align the RG_r color pairs. Next the BTG cells are alternately opened and closed again as in (b) to add the charge packet from the horizontal register cells to the storage cells. Now two RG_r color pairs have been added: $R^2G_r^2$ (f). This operation is repeated for the next line (BG_b color pairs) resulting in (g). Then the cycle is repeated for the next two lines, resulting in (h). Finally

the charge is transported back into the readout register (i). At this stage, the information from 4 sets of RG_rG_bB pixels has been combined in four cells of the readout register. Note that this binning can be extended from 2 x 2 to 2n x 2n binning simply be modifying the pulse patterns.

Evaluation Results

Fig. 5 shows the response of the four color planes (RG_rG_bB) versus exposure time. As can be seen, the linearity is excellent up to saturation and the saturated R,G_r and G_b pixels do not bloom into the B pixels. Also, the green-green differences are very small, indicating good pixel separation (and thus high MTF) not only laterally (over the p^+ channel stops) but also in transport direction (over the blocking gate). The anti-blooming prevents charge from saturating B pixels to leak in vertically neighboring G_r pixels. The maximum charge capacity is 60000 electrons. The deviation from linear is well below 3% up to 80% of saturation.

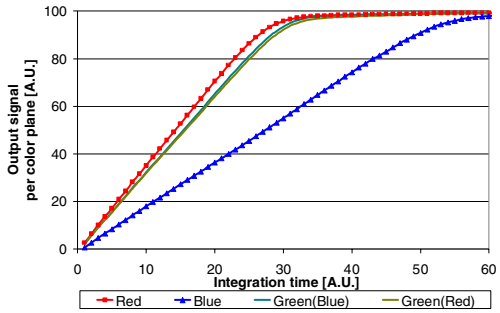

Figure 5. *Linearity measurement: **o**utput signal for RG_rG_bB vs. exposure time*

The pixel array can handle up to 1000 times overexposure. Since both excess electrons and holes can be drained through low-resistance paths (n-substrate for electrons, p^+ channel stops for holes) the image quality in areas next to overexposed pixels is not degraded. Electronic shuttering is achieved in less than 10µs by setting all image electrodes to the low level, and by applying a +5V pulse to the substrate: this implies that the sensor is not the limiting factor in the start-up time for the camera.

Fig. 6 shows the well-balanced RGB response of the pixel in combination with the IR filter required for good color reproduction.

The transport efficiency was measured [3] both for the vertical (pixels, 100kHz) and for the horizontal (register, 25MHz) transport. The efficiency was better than 0.9999995, implying less than 1% loss over 20000 transports (the maximum both in horizontal and in vertical direction).

The angular response is illustrated in Fig. 7. As can be seen, the response is very symmetrical and remains better than 80% up to angles of 25°.

The dark current is 3pA/cm^2 at 20°C, corresponding to 10 electrons per pixel per second.

The output amplifiers have a conversion gain of 40µV/e^- with a noise of 16 electrons at 25MHz pixel frequency, after CDS. This results in a dynamic range of 70dB. Using four output amplifiers, the maximum frame rate is 3 fps.

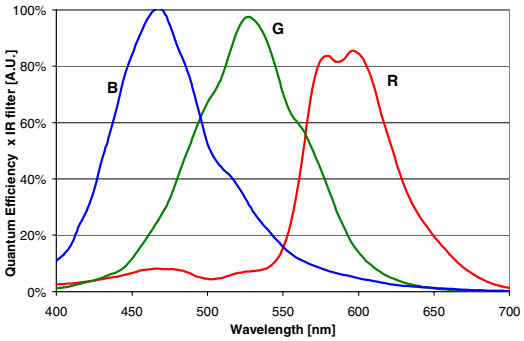

Figure 6. *RGB response combined with IR cut-off filter transmission*

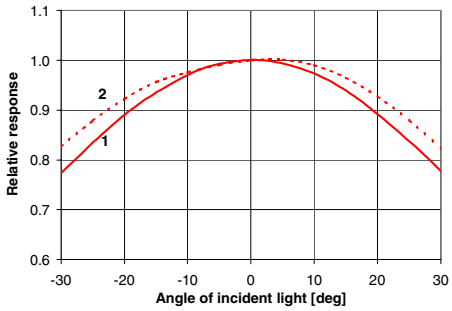

Figure 7. *Angular response. Curve 1 is for rotation along vertical axis, curve 2 for rotation along horizontal axis.*

Fig. 8 shows the response of the blue pixels versus exposure time for the 28M-pixel imager with binning "off" and "on". As can be seen, the sensitivity is increased by a factor of four, and the linearity is not compromised. Detailed measurements show that no charge mixing occurs with binning turned "on", and that the feature is operating correctly [9].

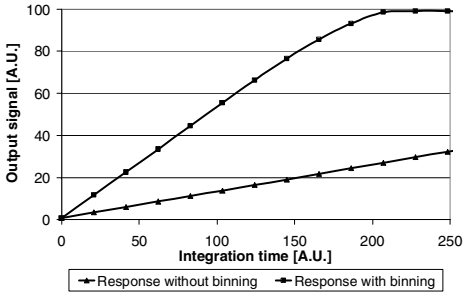

Figure 8. *Linearity measurement: signal form blue pixels with binning "off" and "on".*

Table 1 summarizes the device architecture and performance for the new 33M- and 28M-pixel imagers. Fig. 9 shows a photo of an assembled 33M-pixel sensor in its hermetically sealed package.

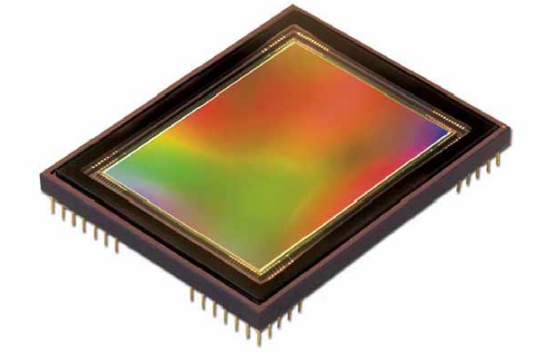

Figure 9. Packaged 33M-pixel CCD imager

Conclusions

Two new imagers for pro-DSC applications were developed: a 33-M pixel imager on 36mm x 48mm format, and a 28M-pixel imager on 44mm x 33mm format. Excellent image quality is obtained by combining highly sensitive pixels of 7.2 µm x 7.2 µm with low dark current with a low-noise amplifier. The dynamic range is 70dB. A novel on-chip RGB-compatible charge binning option was presented as a unique feature to exchange resolution for sensitivity and signal-to-noise ratio.

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Table 1: Summary of Device Architecture and Performance

	33M	**28M**
Application	studio photogr.	social photogr.
Basic Architecture		
CCD concept	full-frame	
Resolution (H x V)	4992 x 6668	6096 x 4560
Pixel Size	7.2 x 7.2µm^2	7.2 x 7.2µm^2
Image area	36 x 48mm^2	44 x 33mm^2
Pixel structure	2-poly, 4-phase	
Readout structure	2-poly, 3-phase	
Readout Modes	1, 2, 4 outputs	
Color filters	RGB Bayer	
RGB Binning option	No	Yes
Operating Conditions		
Pixel integration	0V-8V	
Pixel readout voltage	0V-11V	
Readout register	3V-8V	
Substrate voltage	24V typical	
Electronic shutter	5V pulse	
Outamp supply	20V, 0V	
Pixel Performance		
Charge Capacity	60000 electrons	
Dark Current	3pA/cm^2 [20°C]	
Dark current temp. dependence	doubles per 9°C increase	
Angular response (30% fall-off)	30°	
Output Amplifier		
Conversion factor	40µV/e$^-$	
Bandwidth	130MHz	
Noise after CDS	16e$^-$	
Imaging Performance		
Dynamic Range	70dB	
Maximum frame rate, one output	1 fps	1.1 fps
Maximum frame rate four outputs	4 fps	4.4 fps
Maximum frame rate one amplifier, with 2x2 RGB binning “on”	n/a	3 fps

Author Biography

Jan Bosiers was born in Belgium in 1956. After his studies at the Catholic University of Leuven, Belgium, he worked at the ESAT laboratory of the University on linear CCD imagers. In 1985-1986 he worked as a consultant at the Naval Research Lab in Washington DC, on UV-sensitive backside-illuminated CCD arrays. He joined Philips Research in 1986 to work on CCD imagers for medical and DSC applications. Since 2002, he is R&D Director of DALSA Professional Imaging in Eindhoven, the Netherlands.