Automotive Scene Viewing CMOS Camera System-on-a-Chip with NTSC/PAL Output

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Abstract

This paper describes a highly light-sensitive CMOS camera system-on-a-chip (SOC), targeting automotive scene viewing applications such as backup cameras or side-view mirror replacements. With a paired Bayer CFA, its dual-rolling shutters can integrate for the full duration of a frame (33.3ms/40ms). Its integrated camera functions can process video and generate composite analog video-out (NTSC/PAL).

With a 1/4-inch optical format (VGA resolution) and integrated (single-supply) camera SOC, the total chip size is 6.2mm (H) x 6.5mm (V). The monolithic silicon is packaged in an AEC-Q100-qualified IBGA. The SOC image control functions include automatic black level offset correction, lens shading correction, color recovery and correction, automatic exposure control, and automatic white balance, gamma correction and support for dynamic/static overlay.

Sensor performance and integrated camera features are discussed in this paper.

Introduction

The automotive backup camera is gaining favor as a driver aid in many vehicles today. One of the biggest challenges of this application is good low-light sensitivity. Backup cameras are required to "see" at night with very low illumination. Customers expect the image sensor's low-light sensitivity to outperform that of the human eye. Additionally, the color-processed images are expected to be delivered with a popular and well defined standard— NTSC/PAL composite analog video. Camera manufacturers are also demanding ways to add their own differentiating features like overlay and de-warping. A "marked channel" in the form of an overlay image is typically presented to a driver as a reversing aid. Some camera designers also de-warp images from the fish-eyed backup lens as an additional value-add.

This integrated CMOS camera system-on-a-chip (SOC) is designed specifically for automotive viewing applications. The top priority of low-light sensitivity is achieved by using Micron® DigitalClarity® CMOS imaging pixel technology, known for its low read noise and low dark current. A paired Bayer CFA with interlaced readout enables maximum integration time of a full frame. Its color-processing pipeline can be adjusted to produce good color images with an infra-red cutoff as large as 720nm (enhancing sensitivity in conditions with near-IR radiation). The sensor has a rolling shutter pixel architecture. The pixel is a four-transistor (4T) type, buried photodiode, laid out in a large 5.6µm x 5.6µm pitch with microlens for high fill factor. The device is expected to operate in adverse outdoor environments with wide temperature ranges and noisy (electrical) conditions. It is designed to operate from –40°C to +85°C and supports a single/differential composite NTSC/PAL output for higher noise immunity. It also supports dynamic image overlay with a topology that reduces the overall system solution cost (by routing the overlay data back into the integrated NTSC/PAL encoder). Also, a single power supply (2.8V) eliminates the need for multiple voltage regulators.

Design Considerations

Choice of Sensor Array Parameters

An optical format of 1/4-inch was selected for an optimal tradeoff between the cost of optical elements, the required resolution, and the acceptable sensitivity. The key pixel array parameters are shown in Table 1.

Table 1: Key Array Parameters

Optical Format	¼-Inch (4:3)
Active Imager Size	3.63mm (H) x 2.78mm (V) 4.57mm diagonal
Active Pixels	640H x 480V
Pixel Size	5.6µm x 5.6µm

Sensor Performance

The array readout format is interlaced and the CFA pattern is a modified Bayer pattern (paired Bayer CFA), as shown in Figure 1.

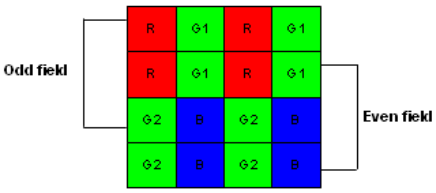

Figure 1: Paired Bayer Pattern

The "paired Bayer" CFA with interlaced readout results in a Bayer stream to the image flow processor (IFP) and provides a maximum integration time capable of spanning a full frame time (33ms for NTSC and 40ms for PAL), resulting in maximum low-light sensitivity. Note that an interlaced readout with a Bayer CFA does not give a stream that can be demosaiced without a field buffer. The common alternative of doubling the frame rate to 60 frames per second and demosaicing a progressively-readout frame (to get a color field) comes with a serious low-light-sensitivity penalty since the maximum integration time is then limited to 1 field (16.66ms/20ms).

Key pixel performance numbers are shown in Table 2.

Table 2: Key Pixel Performance Parameters

Responsivity	**2.8 V/Lux*s**
Fill Factor	70%
QE	48% @ 550nm, with u-lenses
Pixel conversion gain	38μV/e-
Pixel Linear Dynamic Range	**72dB**
Full Well	28K e- (linear-sat)
Read noise (Photodiode to ADC out)	25 e- (at x1 analog gain) 6 e- (at x16 analog gain)
Dark Offset with Temperature	118.7e/s @ 55C 2393e/s @ 85C

The low pixel dark current at high temperatures keeps the dark current shot noise level down and the pixel dynamic range acceptable. Figure 2 shows two images from the sensor at high temperatures.

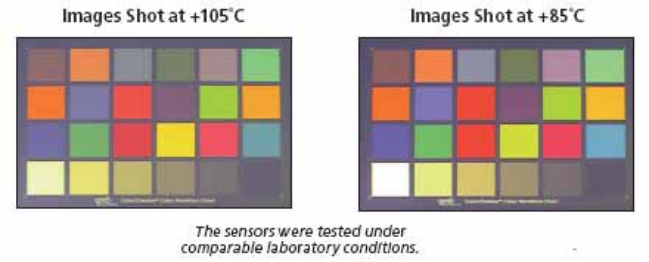

Figure 2: Sensor Performance at High Temperatures

Image Flow Processor (IFP)

The IFP consists of a color-processing pipeline, and a measurement and control logic block (the camera controller). The stream of raw data from the sensor enters the pipeline and undergoes several transformations. Image stream processing starts with conditioning the black level and applying a digital gain. The lens shading block compensates for signal loss caused by the lens. Next, the data is interpolated to recover missing color components for each pixel. The resulting interpolated RGB data passes through the current color correction matrix (CCM), gamma, and saturation corrections, and is formatted for final output. The measurement and control logic continuously accumulate image brightness and color statistics. Based on these measurements, the IFP calculates updated values for exposure time and sensor analog gains that are sent to the sensor core via the control bus. See Figure 3.

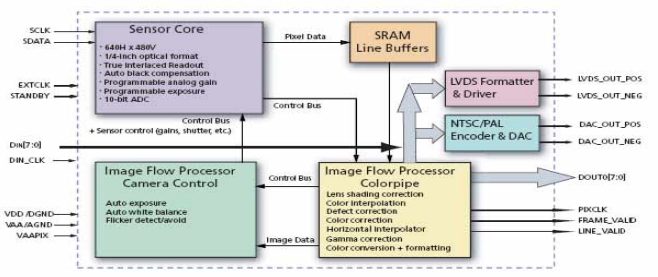

Figure 3: Architectural Overview

Black Level Conditioning

The sensor core black level calibration works to maintain black pixel values at a constant level, independent of analog gain, reference current, voltage settings, and temperature conditions. If this black level is above zero, it must be reduced before color processing can begin. The black level subtraction block in the IFP re-maps the black level of the sensor to zero prior to lens shading correction. Following lens shading correction, the black level addition block provides capability for another black level adjustment. However, for good contrast, this level is normally set to zero.

Lens Shading Correction (LC)

Inexpensive lenses tend to attenuate image intensity near the edges of pixel arrays. Other factors also cause signal and coloration differences across the image. The net result of all these factors is known as lens shading. Lens shading correction (LC) compensates for these differences. Typically, the profile of lens shading induced anomalies across the frame is different for each color component. Lens shading correction is independently calibrated for the color channels.

Interpolation and Aperture Correction

A demosaic engine converts a single color per pixel Bayer data from the sensor into RGB (10 bits per color channel). The demosaic algorithm analyzes neighboring pixels to generate a close approximation for the missing color components. Edge sharpness is preserved as much as possible. Aperture correction sharpens the image by an adjustable amount. Sharpening can be programmed to phase out as light levels drop to avoid amplifying noise.

Color Correction

To obtain good color rendition and saturation, it is necessary to compensate for the differences between the spectral characteristics of the imager color filter array and the spectral response of the human eye. This compensation, also known as color separation, is achieved through linear transformation of the image with a 3 x 3 element color correction matrix. The optimal values for the color correction coefficients depend on the spectra of the incident illumination and can be programmed by the user.

Gamma Correction

To achieve more life-like quality in an image, the IFP includes gamma correction and color saturation control. Gamma correction operates on the luminance component of the image and enables compensation for non-linear dependence of the display device output versus driving signal (e.g., monitor brightness versus CRT voltage).

In addition, gamma correction provides range compression, converting 10-bit luminance input to 8-bit output. Pre-gamma image processing generates 10-bit luminance values ranging from 0 to 896. Piece-wise linear gamma correction utilized in this imager has 10 linear intervals, with end points corresponding to the following input values: XI=0…10={0,16,32,64,128,256,384,512,640,768,896}. For each input value XI, the user can program the corresponding output value YI. YI values must be monotonically increasing.

Support for Dynamic Overlay

The topology in Figure 4 shows how static/dynamic overlay is supported. The digital signal processor (DSP) gets a CCIR-656 stream from the SOC and writes back a CCIR-656 stream with an image overlay to the sensor to be encoded into a composite NTSC/PAL output.

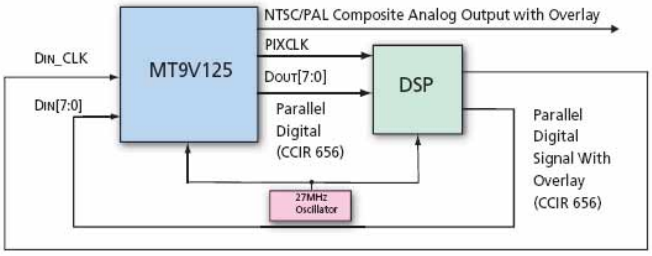

Figure 4: Typical Usage Configuration with Overlay

Packaging

Figure 5 shows a photograph of the image sensor in an AEC-Q100-qualified (level III), 52-pin IBGA package, available in a lead-free option.

Figure 5: 52-Pin IBGA Package

Conclusion

This paper describes a product engineered specifically to address the challenges of automotive scene viewing applications. The overriding need for good low-light sensitivity was met by ensuring the integration time could span a full frame. A large 5.6µm x 5.6µm pixel with superior read noise and low dark current also helped meet these challenges. An integrated solution in the form an SOC meant higher system reliability with lower overall power and component cost. An embedded video encoder and novel architectural support for overlay and de-warp added convenience for a system-level value-add.

References

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Author Biography

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A Progressive Scan PIACCD Image Sensor for 720p HD applications

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Abstract

A progressive scan PIACCD [1] imager having dual output circuit using a new architecture of branch channel HCCD has been developed. The imager can output 5M pixel stills and 720p HD movies with 30fps. The imager doesn't need any extra circuit to adjust the property of one output circuit to that of the other because same color signals are output from either one of two output circuits, on the other hand usual dual output imager whose imaging area is divided on the center must need the extra circuit. And the imager is suitable to reduce noise by CDS because the dual output decreases the data rate by half.

Introduction

To realize CCD image sensors at high-speed data rate, it is the simplest structure that the imager has one horizontal CCD register (HCCD) and one output circuit driven by high frequency as much as 100MHz or more [2]. This type has a difficulty to use the correlated double sampling (CDS) and cannot reduce noises completely. And white noise cannot be reduced by using low-pass filter effectively because the output circuit should have wide bandwidth. As a solution for this problem, the dual output technologies have been developed to decrease the data rate by half. These are classified into two types of HCCD. One has divided channel HCCD. The imaging area is divided on the center, and each area has HCCD. Image signals in the divided two imaging areas are transferred toward opposite directions through HCCDs. This type needs to adjust differences between two output circuits' characteristics, such as gain and offset, to joint two images without a boundary line. The extra adjustment circuits are used to adjust them. But this adjustment is difficult because these characteristics change with temperature fluctuation. And if gain and offset could be adjusted, the noise difference between two output circuits appears on the reproduced image and this type of difference is not adjustable. The other has dual-channel HCCD [3], namely the first HCCD is adjacent to VCCD and the second HCCD is adjacent to the first HCCD. Alternate signal packet chain in a horizontal line is selectively transferred from the first HCCD to the second HCCD, and signals are output from two output circuits. It doesn't need any extra adjustment circuits because it outputs same color signals from either one of two output circuits, and the output data are joined through a white balance processing. But this type has a difficulty in complete transferring from the first HCCD to the second HCCD, because long channel in vertical direction of HCCD prevents the signal charges to transfer from the first HCCD to the second HCCD fast. The remaining charges cause linear blemish, which is a kind of fixed pattern noise, on the reproduced image.

To solve these problems, we developed PIACCD [1] imager having dual output circuits using a new architecture of branch channel HCCD. The imager doesn't need any extra circuits, and it doesn't have any sources causing fixed pattern noise as described later.

Design point of branch channel HCCD

Fig.1 shows the block diagram of the PIACCD imager having dual output circuit using branch channel HCCD. It has a branch electrode on the final transfer stage of serial HCCD and two branch channels (parallel HCCD). Each parallel HCCD have floating diffusion amplifiers and output circuits.

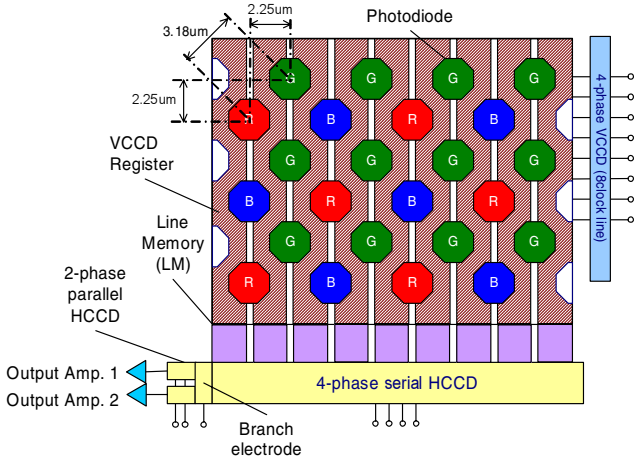

Figure 1*. The block diagram of developed sensor*

Fig.2 shows the schematic diagram around the branch electrode on HCCD. There are two series of electrodes named HS (electrodes in serial HCCD) and HP (electrodes in parallel HCCD), and the branch electrode named HSL. Path of signal charges can be controlled with HP voltage. When HP1=High and HP2=Low, they are transferred under the first HP1 electrode, and vice versa. In this way, charges in the serial HCCD are branched to HP1 and HP2 alternately. As the HP electrodes are driven by half the frequency of that of HS electrodes, the data rate of this imager is equal to the clock frequency of HS.

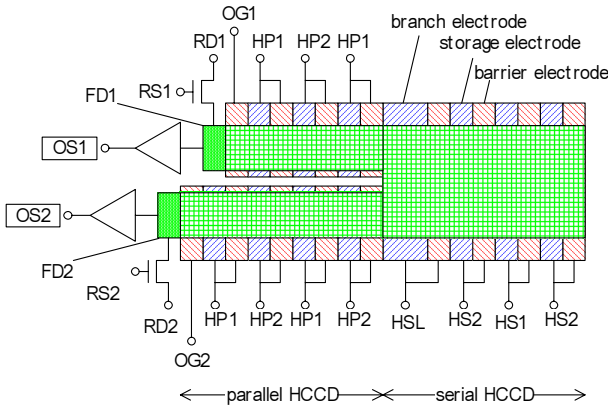

Figure 2. *The schematic diagram around the branch electrode*

The branch channel has difficulty in complete transfer from serial HCCD to parallel HCCD because the transfer period is short, which is half the period of HS clock. To overcome it, we developed two technologies. First, the branch channel layout has designed using new principles of channel layout, and the electric field has been strong enough to transfer on the short time. Second, the voltage applied on the HSL is kept at 0V, not driven by the HS1 pulse. Fig.3 shows the cross section of the branch area with the electric potential profiles. Signal charge in HS2 is transferred to HSL while HS2=L, and then, signal charge in HSL are transferred to HP1 (or HP2) while HP1 (or HP2) =H. If HSL are driven by HS1 pulse, signal charge in HSL are transferred to HP1 (or HP2) while HP1 (or HP2) =H and HS1 =L. Therefore, applying DC voltage on HSL makes it possible to extend the transferring period twice than the time when the electrode is driven by HS1 pulse. We have used these two technologies, and resultantly, charge-transferring efficiency on the branch has realized over 99% on the time (@Signal 50mV).

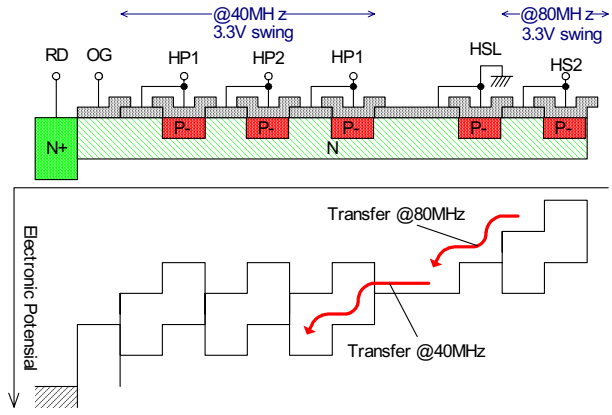

Figure 3. *The cross section around the branch electrode*

High quality 5M pixel still

This imager outputs high-quality stills with high-speed shooting of Max 20fps because it uses the PIACCD technology and the branch channel HCCD technology. PIACCD realizes progressive-scan with a standard double-layer polysilicon, enlarges the saturation voltage by 1.3 times and heightens the sensitivity by 1.3 times than conventional interline transfer CCD. This imager has 2.5M pixels with an interleaved arrangement, and the output images can be reproduced as 5M pixel picture with a pixel interpolate processing [1]. And the imager has a line memory CCD (LM) and a 4-phase HCCD [4]. The 4-phase electrodes can readout column signal charge packets selectively from LM and transfer them into horizontal direction. In case of capturing stills, the output signal sequence of the imager is shown in Fig.4. Since each line has G and R, or G and B in the serial HCCD, after pass the branch area, one parallel HCCD has only G signals and the other has only R or B signals. Therefore, as the differences between two output circuits' characteristics can be absorbed into a white balance processing, this new dual output system doesn't need any extra adjustment circuits.

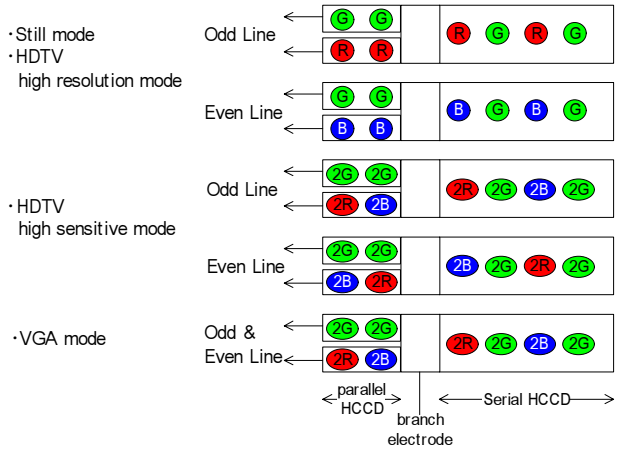

Figure 4. *The output signal sequence*

Fig.5 shows the reproduced images taken by this imager as compared with that taken by the imager using the conventional divided channel HCCD without any adjustment circuits. The image taken by the imager using the branch channel HCCD is very natural in spite of using dual output circuits without any adjustment circuits.

(a) (b)

Figure 5. *Reproduced images taken by (a) imager with branch channel HCCD. (b) imager with conventional divided channel HCCD.*

High quality HDTV and VGA movies

The imager using the branch channel HCCD also produces high quality 720p ('p' means progressive) HD movie and VGA movie. In case of capturing 720p HD movie with 30fps, all signals are read out simultaneously, and signals except for 720 lines are swept away by operating VCCD fast. 720p HD movie can be output by two modes, named high-resolution mode and high-sensitivity mode. The former outputs all signals independently. The latter uses a horizontal charge mixing technology that combines the adjoining same color pixels, and provides twice sensitivity. The output signal sequences are shown in Fig.4. In both modes same color signals are output from either one of two output circuits. In case of capturing VGA movie with 60fps (max 75fps), one of two lines is selected, and as same color signal charges are mixed horizontally, the sensitivity is heightened by 2 times. The signal sequences are shown in Fig.4, and also in this mode, same color signals are output from either one of two output circuits and the differences between two output circuits' characteristics are absorbed into a white balance processing.

The specifications and characteristics of the imager are summarized in Table 1.

Conclusion

A progressive scan PIACCD imager having dual output circuit using a new architecture of branch channel HCCD has been developed. This imager doesn't need any extra circuits to adjust the property of one output circuit to that of the other, and it doesn't have any sources causing fixed pattern noise. Therefore it has completely overcome the disadvantages of conventional dual output image sensors using the divided or the dual channel HCCD, and it will bring the best solution to "Hybrid Camera System" which can take high quality still, HD movie and VGA movie.

Table1. Specifications and characteristics

Device Structure	Progressive Scan PIACCD
Chip Size	6.72mm * 5.67mm
Total Number of Pixels	2.70M
Number of Imaging Pixels	2.49M 4.98M(with pixel Interpolation)
Pixel Spacing (Line Pitch)	4.5um (2.25um)
Imaging Area	5.80mm * 4.35mm
Color Filter	G: Square Lattice R, B: Mosaic
Data Rate	80MHz
Output Signal Formats	(1)Still: 1288(H) * 966(V) * 2 (20fps) (2)720p HD - high-resolution: 1288(H)*724(V)*2 (30fps) - high-sensitivity: 1288(H)*724(V)(Max50fps) (3)VGA: 1288(H)*483(V) (60fps)
Saturation Voltage	750mV
G sensitivity (5100K, 1200cd/m^2,F5.6,1/60s)	440mV
Smear	0.0006% (-104.4dB)

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Author Biography

Makoto Kobayashi was born in Yamagata, Japan, on March 13, 1978. He received the B.S. and M.S. degrees from Tohoku University, Japan, in 2000 and 2002, respectively. He joined Fujifilm Microdevices Co., Ltd. in 2002, and Fuji Photo Film Co., LTD. in 2004. He has been engaged in the research and development of solid-state image sensors.