

CMOS Image Sensors - Past Present and Future

Boyd Fowler, Xinqiao(Chiao) Liu, and Paul Vu
Fairchild Imaging, 1801 McCarthy Blvd. Milpitas, CA 95035 USA

Abstract

In this paper we present an historical perspective of CMOS image sensors from their inception in the mid 1960s through their resurgence in the 1980s and 90s to their dominance in the 21st century. We focus on the evolution of key performance parameters such as temporal read noise, fixed pattern noise, dark current, quantum efficiency, dynamic range, and sensor format, i.e the number of pixels. We discuss how these properties were improved during the past 30 plus years. We also offer our perspective on how performance will be improved by CMOS technology scaling and the cell phone camera market.

Introduction

MOS image sensors are not a new development, and they are also not a typical disruptive technology. MOS image sensors were first devised in the mid 1960's, when the incumbent technology for electronically capturing video was the vidicon tube not the CCD. Vidicon technology was mature with more than 30 years of television development behind it. Although the image quality generated by a vidicon tube was excellent, its size, weight, and lag were disadvantageous for many applications¹. These limitations created the impetus necessary to develop solid state MOS image sensors.

During the 1960's MOS image sensors were used in many applications including optical character recognition, reading aids for the blind, and low resolution 2D cameras. Unfortunately MOS sensors had many problems including both high fixed pattern and temporal noise. CCDs were invented in 1969 and quickly offered better imaging performance than MOS image sensors. This forced MOS image sensors into only a few specialized applications such as spectroscopy.

Throughout the 1970's CCDs dominated the image sensor market, due to their inherently lower FPN. During the early 1980's CCDs were controlled by only a few companies and were produced for only a few applications. This made conditions right for universities and companies to start the exploration of CMOS image sensors, the next generation of MOS image sensors, for various applications. This included applications such as machine vision, hand held video cameras, and space based sen-

sors. CMOS image sensors can integrate sensing and processing on the same chip and have higher radiation tolerance than CCDs. In addition CMOS sensors could be produced by a variety of different foundries. This opened the creative flood gates and allowed people all over the world to experiment with CMOS image sensors.

The 1990's saw the rapid development of CMOS image sensors by universities and small companies. By the end of the 1990's image quality had been significantly improved, but it was still not as good as CCDs. During the first few years of the 21st century it became clear that CMOS image sensor could out-perform CCDs in the high speed imaging market, but that their performance still lagged in other markets. Then, the development of the cell phone camera market provided the necessary capital to improve CMOS image sensors to a point where they out-perform CCDs in many applications today.

Another good description of the history of MOS/CMOS image sensors is presented by Fossum in [2, 3].

In the remainder of this paper we will elaborate on the history of MOS/CMOS image sensors using key performance parameters to track their development. In the next section we present definitions for temporal read noise, fixed pattern noise, dark current, quantum efficiency, dynamic range, and format as they pertain to MOS image sensors. In following three sections we chronicle the invention, resurgence and the present and future of MOS image sensors. Finally we present our conclusions.

Definitions

In this Section we discuss six key parameters that determine an image sensor's performance. This is clearly an oversimplification, because more than six parameters are required to completely characterize an image sensor. In this paper the six parameters that we will focus on are temporal read noise, fixed pattern noise, dark current, quantum efficiency, dynamic range, and sensor format.

In order to simplify the explanation of these parameters we present a simplified model for an image sensor, i.e.

$$Y_{i,j}(t) = g_{i,j}(\eta F_{i,j} t_{int} + I_{i,j}^{dc} t_{int} + N_{i,j}(t)) + O_{i,j}, \quad (1)$$

where $Y_{i,j}$ is the sensor output voltage from pixel (i, j) , η is the quantum efficiency of the sensor, $F_{i,j}$ is the photon flux at pixel

¹For a detailed description of vidicon tubes see [1].

(i, j) , t_{int} is the sensor integration time, $I_{i,j}^{dc}$ is the sensor dark current at pixel (i, j) , $N_{i,j}$ is the temporal read noise, $g_{i,j}$ is the conversion gain of pixel (i, j) , and finally $O_{i,j}$ is the fixed offset voltage of pixel (i, j) .

We define temporal read noise of pixel (i, j) as the RMS variation in $N_{i,j}(t)$. To measure this value the sensor integration time is typically set to zero, i.e. $t_{int} = 0$ and $Y_{i,j}(t)$ is measured multiple times. Temporal read noise is typically reported in electrons(e-) RMS. Temporal read noise consists of thermal and 1/f noise from transistors in the readout path, and detector (photogate or photodiode) reset noise[4].

We define fixed pattern noise (FPN) as the pixel to pixel variation of the sensor when the input signal $F_{i,j}$ is constant for all pixels. In our simple model this implies that FPN consists of two components, offset and gain. The offset FPN is caused by dark current variation and transistor mismatch, i.e. the pixel to pixel variations in $g_{i,j}(I_{i,j}^{dc}t_{int}) + O_{i,j}$. Gain variation is caused by variation in effective pixel size and conversion gain, i.e. $g_{i,j}$. We will define offset FPN as the peak to peak variation from pixel to pixel divided by the sensor full scale output, and we define gain FPN as $(\max g_{i,j} - \min g_{i,j}) / \overline{g_{i,j}}$ where $\overline{g_{i,j}}$ is the average sensor gain. See [5] for detailed discussion of FPN in MOS image sensors.

Dark current $I_{i,j}^{dc}$ is the photodetector leakage current. It is typically measured as a function of integration time and temperature when $F_{i,j} = 0$. It is often reported in units of pA/cm² at a specific operating temperature. Dark current consists of both Shockley–Hall–Read (SHR) generation and diffusion currents[6]. It is very sensitive to temperature and silicon defect density. For example, the dark current doubling rate of a MOS image sensor is typically between 6-12°C at room temperature.

Quantum efficiency η is defined as the ratio between the number of collected electron/hole pairs to the number of incident photons at a specific wavelength. The quoted quantum efficiency is typically the maximum achieved over the visible spectrum.

Dynamic range is defined as the maximum non-saturating signal divided by the temporal read noise. For example, if the average sensor conversion gain $\overline{g_{i,j}} = 2\mu\text{V/e-}$ and the maximum output signal is 1V and the sensor temporal read noise is 50e-RMS, then the dynamic range of the sensor is $500000/50 = 10000$, i.e. 80dB. Finally, sensor format is the number of pixels in an image sensor.

Invention of the MOS Image Sensor

Research on solid state image sensors began in the mid 1960's. The first MOS integrating solid state image sensor was developed at Fairchild Semiconductor in Palo Alto, California by G. Weckler in 1967[7]. He developed a MOS passive pixel

architecture as shown in Figure 1 that used a reverse biased photodiode to integrate photogenerated charge, connected to a single pchannel MOS transistor to individually access each pixel in a linear array. The photodiode is read out by turning on the MOS access transistor and transferring charge from the photodiode to a column amplifier via the column bit line. During this process the photodiode is also reset to fixed voltage determined by the column level amplifier. Typically a capacitive transimpedance amplifier is used at the column level for passive pixel sensors. Between readout periods the photodiode is always integrating photocharge. This development dramatically increased the sensitivity of MOS image sensors compared with non-integrating photoresistive sensors.

Quickly, researchers at Plessey, Stanford University, University of Waterloo, and Nippon Electric Company started development of MOS image sensors. In 1968 P. Noble at Plessey in Northamptonshire England proposed the MOS active pixel architecture[8]. This pixel architecture, shown in Figure 2, uses a pchannel MOS transistor to buffer the photodiode voltage. This circuit trades-off higher sensor speed and lower temporal read noise for smaller pixel fill factor, i.e. the ratio of photodiode area to the pixel area. The photodiode is reset by turning on **M1**, which forces the voltage across the photodiode to **VDD**. The photodiode voltage is readout by turning on **M3** and using **M2** as a source follower. Just like the MOS passive pixel architecture, between readout/reset periods the photodiode is always integrating photocharge. Other researchers at Plessey and at the University of Waterloo in Canada also worked on the MOS active pixel architecture[9, 10, 11] during late 1960's and early 1970's.

At the same time researchers at Stanford University were working on MOS passive pixel image sensors for aiding the blind to read standard printed text[12, 13, 14]. This research was commercialized into the Optacon in the early 1970's.

In Japan, Nippon Electric Company (NEC) was also developing MOS passive pixel image sensors for line scan applications[15] in the early 1970's.

The performance of early MOS image sensors was limited by offset fixed pattern noise caused by MOS transistor threshold and gate-to-source overlap capacitance variation. For example a typical MOS image sensor had about 5% full scale (FS) offset fixed pattern noise. That corresponds to about $\pm 300\text{mV}$ of pixel to pixel variation under dark conditions.

Just after the development of the MOS image sensors, CCDs were conceived by W. S. Boyle and G. E. Smith at AT&T in September of 1969[16]. CCD image sensors quickly evolved to become the prevailing technology for visible solid-state imaging, mainly because MOS image sensors could not match their imaging performance. Moreover, CCDs achieved an order of magnitude lower offset fixed pattern noise than contemporary

MOS image sensors. This caused research on MOS image sensors to almost stop until the early 1980's.

Resurgence of the MOS Image Sensor

By the early 1980's CCD technology had improved significantly. Dark current had been reduced to 10s of pA/cm² by using pinned photodiode and multi-phase pinned buried channel devices, temporal read noise had been reduced to 10s of electrons RMS via correlated double sampling (CDS), and quantum efficiency (QE) had been improved to greater than 90% via backside illumination[17, 18, 19]. Although CCDs had higher performance than MOS image sensors there were still reasons to develop MOS image sensor technology. Specifically, CCDs were controlled by a few companies, limiting access to the technology, CCDs have poor radiation tolerance, and sensing and processing could not be integrated on the same chip.

In the early 1980's researchers at Hitachi in Japan[20, 21, 22, 23] and at the University of Linkoping in Sweden[24, 25]

started investigating MOS sensors as an alternative to CCDs. Both groups used a passive pixel architecture. The Hitachi group focused on NTSC format, 492 × 388 pixel, 2-D sensors for portable video camera applications. They reduced the sensor offset FPN to less than 0.03% of the full scale output (FS), and increased the dynamic range to 61dB. Now temporal read noise and dark current were the dominate performance limitations in MOS image sensors, when compared with CCDs.

R. Forchheimer and his group at the University of Linkoping were interested in developing smart sensors for industrial inspection applications. They developed a smart sensor technology that allowed them to integrate a 1-D photodiode array with an analog to digital converter (ADC) and a simple signal processor. This work was commercialized by Integrated Vision Products AB (IVP) in Linkoping Sweden. Throughout the 1980's and 1990's IVP developed smart MOS sensors for industrial inspection, food sorting, quality control, and robotic vision. Although passive pixel sensors suffer from poor temporal read noise and high dark current, this limitation is not a serious problem in machine vision applications because illumination is well controlled and integration times are short.

Work at the University of Linkoping did not go unnoticed, and by the end the 1980's researchers at the University of Edinburgh in Scotland were also developing MOS image sensors. Using a passive pixel architecture, P. Denyer *et al.* focused on low cost high volume single chip 2-D cameras[26, 27, 28]. These cameras contained a 2-D sensor, an ADC, and enough digital logic to perform various camera control functions. In the early 1990's this work spawned VLSI Vision Ltd. (Vision) in Edinburgh Scotland, and this group continued work in this area until they were acquired by ST Microelectronics in 1999. Currently this same group is developing CMOS image sensors for cell phone camera applications. Between the late 1990's and now, image quality requirements forced Vision/ST to change from passive pixel sensors to 3T active pixel sensors, and finally to 4T active pixel sensors with pinned photodiodes[29, 30]. These changes enabled temporal read noise to be reduced from 100s of electrons RMS to 14e- RMS, dark current to be reduced from more than 1nA/cm² to 40pA/cm² at room temperature, and sensor formats increased from 16k pixels to greater than 1.3M pixels.

In the early 1990's another group of researchers at JPL in Pasadena California, started to investigate CMOS image sensors for space applications[2, 31, 32, 3, 33, 34, 35]. CMOS image sensors typically have much higher radiation tolerance than CCD image sensors, making them much more suitable for space applications. Unlike contemporary research in Japan and Europe, Fossum *et al.* focused on active pixel sensors with either photodiode or photogate detectors. This work was commercialized by Photobit in the mid 1990's. Photobit was acquired by

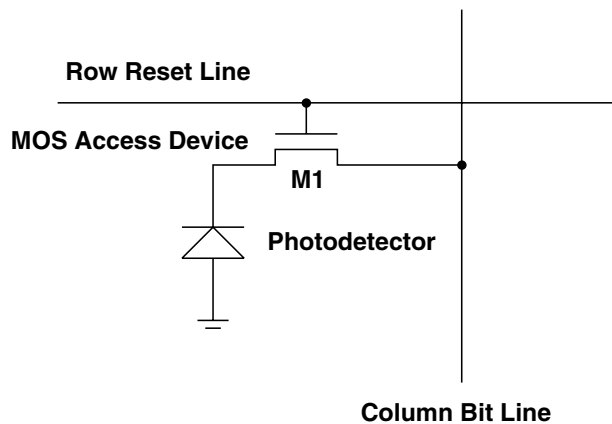


Figure 1. Passive Pixel

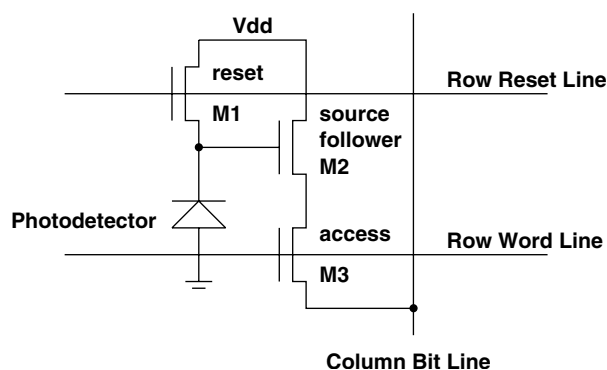


Figure 2. Active Pixel

Micron Technology in 2001, and currently this same group is also developing CMOS image sensors for cell phone cameras. Researchers at JPL are still investigating high-end CMOS image sensors for space and military applications[36, 37]. This work has produced 2-D photogate sensors that achieve 5e- RMS temporal readout noise and 2-D photodiode sensors with 109dB of intrascene dynamic range.

In 1992 researchers at Stanford University in Palo Alto California started to investigate CMOS image sensors with pixel level ADC[38, 39, 40, 41]. This research was focused on understanding the trade-offs associated with sensor dynamic range, frame rate, interface simplicity, pixel level processing, and image quality. Commercialization of this work was performed by Pixel Devices and Pixim in the late 1990's. Pixel Devices focused on developing ultra low noise high sensitivity linear image sensors with pixel level processing for industrial applications[42, 43, 44]. Pixel Devices was acquired by Agilent Technologies in 2003. Pixim developed ultra wide dynamic 2-D sensors for surveillance applications. Currently Pixim is still an independent company that produces sensors for high dynamic range surveillance applications. The work at Stanford and Pixim produced 2-D sensors with a dynamic range of 96dB and frame rates up to 10K frames/sec on a 352×288 sensor, i.e. 1Gpixel/sec. The work at Pixel Devices produced linear CMOS image sensors with temporal readout noise of 1.4e- RMS and a dynamic range of 96dB at 2.7Klines/sec.

In addition to the work already discussed, researchers at the California Institute of Technology, Harvard University, MIT, Canon, IMEC, AT&T, Rockwell, and others were also active in the development of CMOS image sensors during the 1980's and 1990's[45, 46, 47, 48, 49, 50, 51, 52, 53, 54].

At the end of the 1990's and during the first few years of 21st century it became clear that CMOS image sensors were quickly approaching the performance levels of CCDs in many markets, and they had already surpassed the performance of CCDs in high speed industrial imaging and high radiation imaging[55].

CMOS Image Sensors Today and Tomorrow

In the 1990's most CMOS Image Sensors (CIS) were associated with low cost toys due to their inferior quality, but current CIS rival or surpass the performance of most CCDs. The rapid development of the cell phone camera market, i.e. mobile imaging, has been the driving force behind these technology advancements.

Most of the challenges in mobile imaging arise from the demanding size, cost, and imaging requirements under low light level conditions. As customers demand higher resolutions, pixel size must be reduced. Currently state of the art pixel pitch ranges from $2\mu\text{m}$ to $2.5\mu\text{m}$, where the floating diffusion (FD), reset,

source follower and row selection transistors are shared among 4 pixels ($1.75T/\text{pixel}$) [56, 57, 58]. Mainstream CIS are fabricated using a $0.18\mu\text{m}$ CMOS technology, and by the end of 2006 $0.13\mu\text{m}$ CIS technology will be in production. Process technology scaling is enabling smaller pixels and higher resolution at an almost fixed cost for the digital still and cell phone camera markets.

The introduction of the pinned photodiode has dramatically improved the performance of CIS under low light conditions. The pinned photodiode was developed to reduce lag in CCDs, but today it is used to reduce dark current and temporal read noise. It is constructed using a fully depleted n layer sandwiched between two p layers, i.e. the p surface pinning layer and the p substrate. Dark current is typically reduced by two orders magnitude due to the isolation of generation sites at the surface of the photodiode, and true CDS is also enabled by the pinned photodiode. As a result, state of the art CIS has much lower dark current ($< 50\text{pA}/\text{cm}^2$), lower temporal read noise (5–8e- RMS, [56, 57]), and lower offset FPN ($< 0.01\%FS$ [56]). Pinned photodiodes typically have a peak QE of approximately 50%.

The development of pinned photodiodes in low voltage CMOS process, however, was not an easy task. Due to the limited supply voltage, complete charge transfer from photodiode to the floating diffusion is a challenge as the potential barrier and/or pocket underneath the transfer gate could result in image lag [59]. Moreover, the requirements of maintaining a large full well capacity, high responsivity, high QE, and low crosstalk while continuously shrinking pixel size, demand constant process engineering and design trade-off optimization. [58, 60, 61]

In addition to low power consumption and system integration, high speed and low noise readout are also advantages of CIS over CCD's. In [62], a 1920×1440 CIS is presented that operates at 180 frames/sec (6.0Gbps) with only 5.2e- RMS of temporal read noise and 580 mW of power dissipation; and in [63], a CIS with sub-electron temporal read noise was demonstrated that potentially could be used for photo counting.

CIS are quickly becoming ubiquitous in almost every market including industrial, scientific, medical, and defense imaging. Even digital still cameras (DSC) and camcorders are switching from CCDs to CIS [64]. Intelligent transport systems and automotive "scene processing" applications are starting to rely on CIS [65]. In addition, numerous experiments have been reported where CIS are used for *in vitro* and *in vivo* live cell imaging, for studying bio-luminescence, and for DNA sequencing [66, 67].

Conclusions

The performance of MOS/CMOS image sensors has continuously improved since their inception in the late 1960's.

Moore's law and the capital generated by the cell phone camera market promise to keep this trend going many years to come. In the following six figures we graph some of the improvements in MOS/CMOS image sensors over the past 30 plus years. The points in each graph represent reported data and the solid line is the least squares linear fit to the data. These figures are incomplete and do not show correlations between parameters or trade-offs between parameters, but they do show the general trends. Figure 3 shows how offset FPN as been reduced as a function of time to a level where it is unnoticeable today. Figure 4 shows

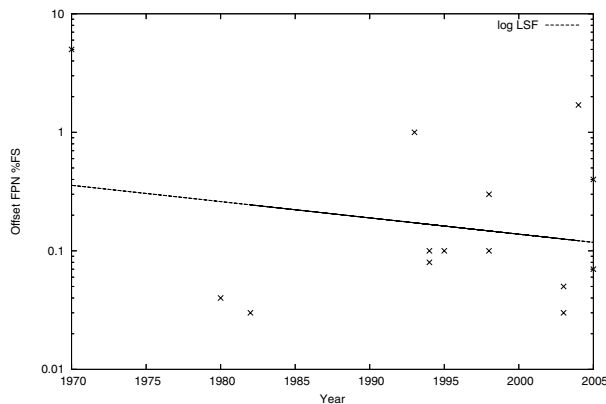


Figure 3. MOS/CMOS Image Sensor Offset FPN

how temporal read noise has been reduced as a function of time from 100s of e- RMS to less than 10e- RMS. This has been enabled by CMOS technology shrinking and the pinned photodiode. Figure 5 shows how dynamic range has been increased as

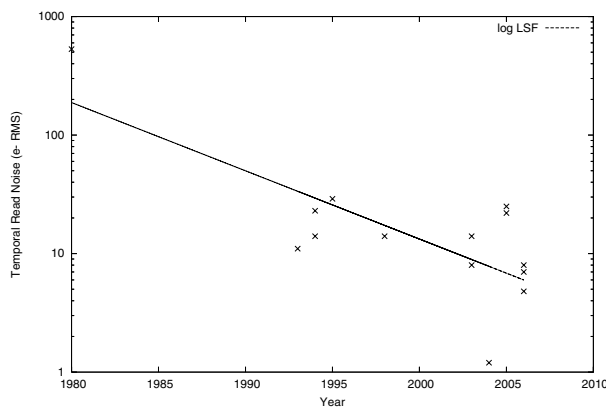


Figure 4. MOS/CMOS Image Sensor Temporal Read Noise

a function of time to over 100dB, but this graph also shows that

60-70dB is still a typical value for most applications. Figure 6

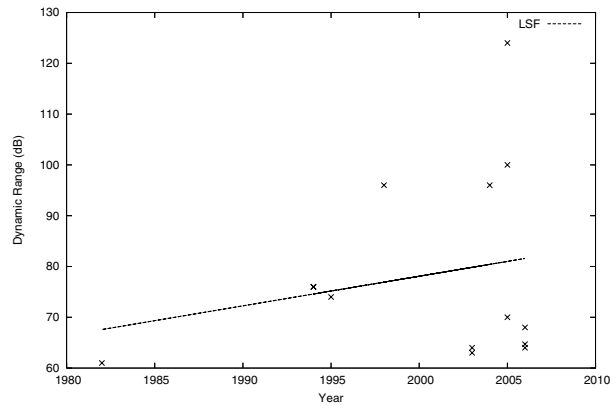


Figure 5. MOS/CMOS Image Sensor Dynamic Range

shows how dark current has been decreased as a function of time from 100s of nA/cm² to 10s of pA/cm² by using pinned photodiodes. Figure 7 shows how quantum efficiency has stayed con-

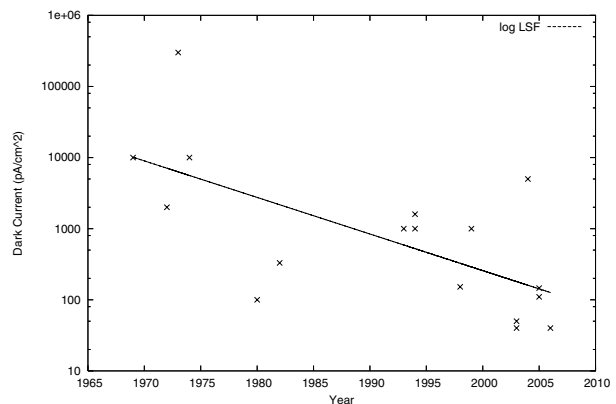


Figure 6. MOS/CMOS Image Sensor Dark Current

stant or decreased slightly as a function of time. This is due to reductions in pixel size and the reflective limitation caused by the SiO₂ silicon interface[68]. Clearly the next step for CIS is backside illumination[69]. Figure 8 shows how the number of pixels in a MOS/CMOS image sensor has increased from 10s in the 1960's to over 10 million in the 21st century.

Acknowledgments

We would like to thank David Wen, Steve Mims, Brett Frymire, and Dan Laxson for their helpful comments.

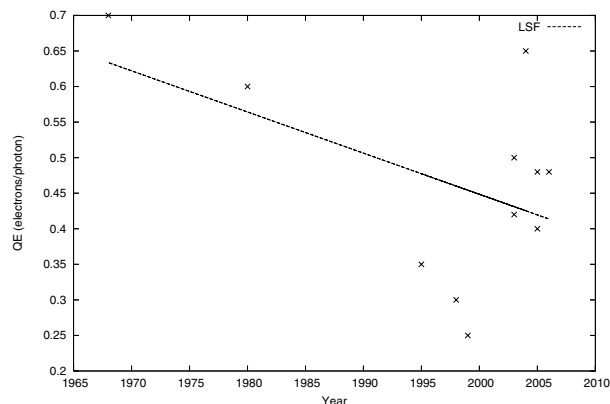


Figure 7. MOS/CMOS Image Sensor Quantum Efficiency

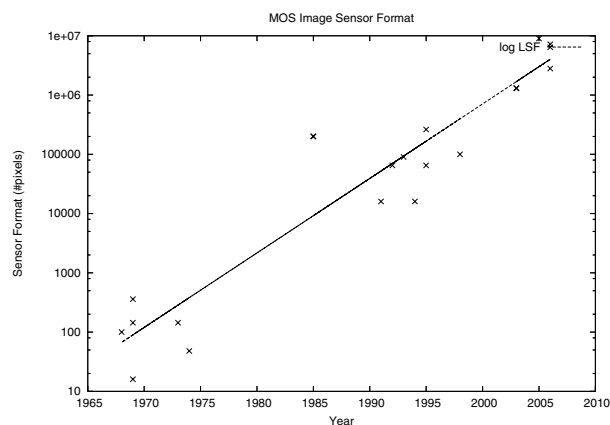


Figure 8. MOS/CMOS Image Sensor Format

References

- [1] S. Donati, *Photodetectors: Devices, Circuits, and Applications*, Prentice Hall PTR, 2000.
- [2] E. Fossum, "Active Pixel Sensors: are CCD's dinosaurs," in *Proceedings of SPIE*, pp. 2–14, (San Jose), February 1993.
- [3] E. Fossum, "CMOS Image Sensors: Electronic Camera On A Chip," in *IEEE IEDM Technical Digest*, December 1995.
- [4] H. Tian, B. Fowler, and A. El Gamal, "Analysis of Temporal Noise in CMOS APS," in *Proceedings of SPIE*, vol. 3649, (San Jose), January 1999.
- [5] A. El Gamal, B. Fowler, and H. Min, "Modeling and Estimation of FPN Components in CMOS Image Sensors," in *Proceedings of SPIE*, vol. 3301, (San Jose), January 1998.
- [6] R. Muller and T. Kamins, *Device Electronics for Integrated Circuits*, Wiley, 1986.
- [7] G. Weckler, "Operation of p-n Junction Photodectors in a Photon Flux Integration Mode," *IEEE Journal of Solid State Circuits* **2**(3), pp. 65–73, 1967.
- [8] P. J. W. Noble, "Self-Scanned Silicon Image Detector Arrays," *IEEE Transactions on Electron Devices* **15**, pp. 202–209, April 1968.
- [9] S. G. Chamberlain, "Photosensitivity and Scanning of Silicon Image Detector Arrays," *IEEE Journal of Solid State Circuits* **4**(6), pp. 333–342, 1969.
- [10] P. W. Fry, P. J. W. Noble, and R. J. Rycroft, "Fixed-Pattern Noise in Photomatrices," *IEEE Journal of Solid State Circuits* **5**(5), pp. 250–254, 1970.
- [11] S. G. Chamberlain and V. K. Aggarwal, "Photosensitivity and Characterization of a Solid-State Integrating Photodetector," *IEEE Journal of Solid State Circuits* **7**(2), pp. 202–204, 1972.
- [12] J. S. Brugler, J. D. Meindl, J. D. Plummer, P. J. Salsbury, and W. T. Young, "Integrated Electronics for a Reading Aid for the Blind," *IEEE Journal of Solid State Circuits* **4**, pp. 304–312, December 1969.
- [13] J. D. Plummer and J. D. Meindl, "MOS Electronics for a Portable Reading Aid for the Blind," *IEEE Journal of Solid State Circuits* **7**, pp. 111–119, April 1972.
- [14] S. Horiuchi and R. D. Melen, "A 24×6 Interlaced-Scan MOS Image Sensor," *IEEE Journal of Solid State Circuits*, pp. 286–288, August 1973.
- [15] T. Ando, Y. Ishihara, and T. Akahoshi, "New Solid-State Image Scanner Capable of Random Positioning," *IEEE Journal of Solid State Circuits* **7**, pp. 251–253, June 1972.
- [16] W. Boyle and G. Smith, "Charge Coupled Semiconductor Devices," *Bell Systems Technical Journal* **49**, p. 587, 1970.
- [17] R. H. Walden *et al.*, "The buried channel charge coupled device," *Bell Systems Technical Journal Briefs*, p. 1635, 1972.
- [18] M. Cutler and other. U.S Patent No. 3,781,574, 1973.
- [19] M. Blouke *et al.*, "Three-phase, backside-illuminated 500×500 CCD," in *ISSCC Digest of Technical Papers*, (San Francisco), February 1978.
- [20] S. Ohba *et al.*, "MOS Area Sensor: Part II – Low-Noise MOS Area Sensor with Antiblooming Photodiodes," *IEEE Transactions on Electron Devices* **27**, pp. 1682–1687, August 1980.
- [21] M. Aoki *et al.*, "2/3-Inch Format MOS Single-Chip Color Imager," *IEEE Transactions on Electron Devices* **29**, pp. 745–750, April 1982.
- [22] S. Ohba *et al.*, "Vertical Smear Noise Model for an MOS-Type Color Imager," *IEEE Transactions on Electron Devices* **32**, pp. 1407–1410, August 1985.
- [23] H. Ando *et al.*, "Design Consideration and Performance

- of a New MOS Imaging Device," *IEEE Transactions on Electron Devices* **32**, pp. 1484–1489, August 1985.
- [24] R. Forchheimer and A. Ödmark, "A Single Chip Linear Array Processor," in *Proceedings of SPIE*, (Geneva), April 1983.
- [25] R. Forchheimer, P. Ingelhart, and C. Jansson, "MAPP2200, a Second Generation Smart Optical Sensor," *SPIE*, 1992.
- [26] P. Denyer, D. Renshaw, G. Wang, M. Lu, and S. Anderson, "On-Chip CMOS Sensors for VLSI Imaging Systems," in *VLSI-91*, 1991.
- [27] P. Denyer, D. Renshaw, G. Wang, and M. Lu, "A Single-Chip Video Camera with On-Chip Automatic Exposure Control," in *ISIC-91*, 1991.
- [28] P. Denyer, D. Renshaw, G. Wang, and M. Lu, "CMOS Image Sensors For Multimedia Applications," in *CICC93*, 1993.
- [29] S. G. Smith *et al.*, "A Single-Chip CMOS 306 × 244-Pixel NTSC Video Camera and a Descendant Coprocessor Device," *IEEE Journal of Solid State Circuits* **33**, pp. 2104–2111, December 1998.
- [30] K. Findlater *et al.*, "SXGA Pinned Photodiode CMOS Image Sensor in 0.35 μm Technology," in *2003 ISSCC Digest of Technical Papers*, (San Francisco, CA), February 2003.
- [31] S. Mendis *et al.*, "Progress in CMOS Active Pixel Image Sensors," in *Proceedings of SPIE*, pp. 19–29, (San Jose), February 1994.
- [32] E. Fossum *et al.*, "A 256 × 256 Active Pixel Image Sensor with Motion Detection," in *ISSCC95 Technical Digest*, February 1995.
- [33] R. Panicacci *et al.*, "128 Mb/s Multiport CMOS Binary Active-Pixel Image Sensor," in *ISSCC96 Technical Digest*, February 1996.
- [34] O. Yadid-Pecht, B. Mansoorian, E. R. Fossum, and B. Pain, "Optimization of Noise and Responsivity in CMOS Active Pixel Sensor for Detection of Ultra Low Light Levels," in *Proceedings of SPIE*, vol. 3019, (San Jose), January 1997.
- [35] O. Yadid-Pecht and E. Fossum, "Wide Intra-scene Dynamic Range CMOS APS Using Dual Sampling," *IEEE Transactions on Electron Devices* **44**, pp. 1721–1723, October 1997.
- [36] B. Pain *et al.*, "Analysis and Enhancement of Low-light-level Performance of Photodiode-type CMOS Active Pixel Imagers Operated with Sub-threshold Reset," in *1999 IEEE Workshop on CCDs and AIS*, (Nagano), June 1999.
- [37] B. Pain *et al.*, "Reset Noise Suppression in Two-Dimensional CMOS Photodiode Pixels through Column-based Feedback-Reset," in *2002 IEDM*, pp. 809–811, 2002.
- [38] B. Fowler, A. El Gamal, and D. X. D. Yang, "A CMOS Area Image Sensor with Pixel-Level A/D Conversion," in *ISSCC Digest of Technical Papers*, (San Francisco), February 1994.
- [39] D. Yang, B. Fowler, and A. El Gamal, "A 128 × 128 CMOS Image Sensor with Multiplexed Pixel Level A/D Conversion," in *CICC96*, 1996.
- [40] D. X. D. Yang, A. E. Gamal, B. Fowler, and H. Tian, "A 640 × 512 CMOS Image Sensor with Ultrawide Dynamic Range Floating-Point Pixel-Level ADC," *IEEE Journal of Solid State Circuits* **34**, pp. 1821–1834, December 1999.
- [41] S. Kleinfelder, S. Lim, X. Liu, and A. E. Gamal, "A 10,000 Frames/s CMOS Digital Pixel Sensor," *IEEE Journal of Solid State Circuits* **36**, pp. 2049–2059, December 2001.
- [42] B. A. Fowler, M. D. Godfrey, J. Balicki, and J. Canfield, "Low-noise Readout Using Active Reset for CMOS APS," in *Proceedings of SPIE*, vol. 3965, pp. 126–135, (San Jose), January 2000.
- [43] B. A. Fowler, J. Balicki, D. How, and M. D. Godfrey, "Low-FPN High-gain Capacitive Transimpedance Amplifier for Low-noise CMOS Image Sensors," in *Proceedings of SPIE*, vol. 4306, pp. 68–77, (San Jose), January 2001.
- [44] B. A. Fowler, J. Balicki, D. How, S. Mims, J. Canfield, and M. D. Godfrey, "An Ultra Low Noise High Speed CMOS Linescan Sensor for Scientific and Industrial Applications," in *Proceedings of SPIE*, vol. 5301, pp. 222–231, (San Jose), January 2004.
- [45] C. Mead, "A Sensitive Electronic Photoreceptor," in *1985 Chapel Hill Conference on VLSI*, (Chapel Hill), 1985.
- [46] C. Mead, *Analog VLSI and Neural Systems*, Addison-Wesley, 1989.
- [47] N. Tanaka *et al.*, "A 310k Pixel Bipolar Imager (BASIS)," in *ISSCC Digest of Technical Papers*, (San Francisco), February 1989.
- [48] M. Gottardi, A. Sartori, and A. Simoni, "POLIFEMO: An Addressable CMOS 128 × 128 - Pixel Image Sensor with Digital Interface," tech. rep., Istituto Per La Ricerca Scientifica e Tecnologica, 1993.
- [49] W. Yang, "A Wide-Dynamic-Range Low-Power Photosensor Array," in *ISSCC Digest of Technical Papers*, (San Francisco), February 1994.
- [50] M. Loinaz and B. Wooley, "A CMOS Multi-Channel IC For Pulse Timing Measurements with 1mV Sensitivity," in *ISSCC Digest of Technical Papers*, (San Francisco), February 1995.
- [51] A. Dickinson, S. Mendis, D. Inglis, K. Azadet, and E. Fossum, "CMOS Digital Camera With Parallel Analog-to-Digital Conversion Architecture," in *1995 IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors*, April 1995.
- [52] B. Dierickx *et al.*, "Random addressable active pixel image

- sensors," *Proceedings of SPIE*, pp. 2–7, 1996.
- [53] S. Decker, R. D. McGrath, K. Brehmer, and C. G. Sodini, "A 256×256 CMOS Imaging Array with Wide Dynamic Range Pixels and Column-Parallel Digital Output," *IEEE Journal of Solid State Circuits* **33**(12), pp. 2081–2091, 1998.
- [54] L. J. Kozlowski, "Theoretical Basis and Experimental Confirmation: Why a CMOS Imager is Superior to a CCD," in *Proceedings of SPIE*, vol. 3698, pp. 388–396, July 1999.
- [55] J. Bogaerts and B. Dierickx, "Total Dose Effects on CMOS Active Pixel Sensors," in *Proceedings of SPIE*, vol. 3965, pp. 157–167, (San Jose), January 2000.
- [56] S. Y. others, "A 1/1.8-inch 6.4MPixel 60frames/s CMOS Image Sensor with Seamless Mode Change," in *ISSCC Digest of Technical Papers*, (San Francisco), February 2006.
- [57] Y. Kim *et al.*, "1/2-inch 7.2MPixel CMOS Image Sensor with 2.25m Pixels Using 4-Shared Pixel Structure for Pixel-Level Summation," in *ISSCC Digest of Technical Papers*, (San Francisco), February 2006.
- [58] G. Agranov *et al.*, "Optical-electrical characteristics of small, sub-4um and sub-3um pixels for modern CMOS Image Sensor," in *2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, (Nagano, Japan), June 2005.
- [59] I. Inoue, N. Tanaka, H. Yamashita, T. Yamaguchi, H. Ishiwata, and H. Ihara, "Low-Leakage-Current and Low-Operating-Voltage Buried Photodiode for a CMOS Imager," *IEEE Trans. on Electron Devices* **50**, pp. 43–47, January 2003.
- [60] A. Krymski and K. Feklistov, "Estimates of Scaling of Pinned Photodiodes," in *2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, (Nagano, Japan), June 2005.
- [61] H. Kwon, I. Kang, B. Park, J. Lee, and S. Park, "The analysis of dark signals in the CMOS APS Imagers from the characterization of test structures," *IEEE Trans. on Electron Devices* **51**, pp. 178–184, February 2004.
- [62] Y. Nitta *et al.*, "High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor," in *ISSCC Digest of Technical Papers*, (San Francisco), February 2006.
- [63] N. Kawai and S. Kawahito, "A Low-Noise Signal Readout Circuit Using Double-Stage Noise Cancelling Architecture for CMOS Image Sensors," in *2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, (Karuizawa, Nagano, Japan), June 2005.
- [64] G. Meynants *et al.*, "A 9 Megapixel APS-size CMOS image sensor for digital photography," in *2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, (Nagano, Japan), June 2005.
- [65] N. Bock *et al.*, "A Wide-VGA CMOS Image Sensor with Global Shutter and Extended Dynamic Range," in *2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, (Nagano, Japan), June 2005.
- [66] D. C. Ng, M. Matsuo, T. Tokuda, K. Kagawa, M. Nunoshita, and J. Ohta, "In vitro and in vivo on-chip biofluorescence imaging using a CMOS image sensor," in *Proceedings of SPIE*, January 2006.
- [67] H. Eltoukhy, K. Salama, A. E. Gamal, M. Ronaghi, and R. Davis, "A 0.18um CMOS 10-6lux Bioluminescence Detection SoC," in *ISSCC Digest of Technical Papers*, (San Francisco), February 2004.
- [68] M. Born and E. Wolf, *Principles of Optics*, Pergamon Press, New York, 1986.
- [69] B. Pain *et al.*, "A Back-Illuminated Megapixel CMOS Image Sensor," in *2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, (Karuizawa, Nagano, Japan), June 2005.

Author Biography

Boyd Fowler received his M.S.E.E. and Ph.D. degrees from Stanford University in 1990 and 1995 respectively. After finishing his Ph.D. he stayed at Stanford University as a research associate in the Electrical Engineering Information Systems Laboratory until 1998. In 1998 he founded Pixel Devices International in Sunnyvale California. Presently he is CTO and VP of Technology at Fairchild Imaging. He has authored numerous technical papers and patents. He's current research interests include CMOS image sensors, low noise image sensors, noise analysis, and data compression.

Xinqiao (Chiao) Liu received the M.S., Ph.D. degrees in Electrical Engineering from Stanford University in 1997, 2002, respectively. Prior joining Fairchild Imaging Inc. in 2003, he was with Canesta Inc (Sunnyvale, CA), developing 3D range sensors. Dr. Liu's research interest includes low light level imaging technologies and 3D sensors.

Paul Vu is manager of the Sensor Design group at Fairchild Imaging, and directs the design and development efforts of new CCD and CMOS image sensors. He has been intimately involved in the development of advanced image sensors for space and scientific applications since 1982.