The Recent Progress on Field Emission Displays

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Abstract

Field emission displays (FEDs) including Surface-conduction Electron-emitter Displays (SEDs) have been showing tremendous progress and become attractive nanoelectronic technology for a new generation of flat panel displays. However, there are important limitations of their reliability and efficiency in FEDs and SEDs, mainly attributed to the emitters. The Transfer Mold emitters, the carbon nanotube emitters and the Si nano crystalline emitters have been the candidates for getting and controlling the emitter structures. In this paper, the recent progress and the technical issues on FEDs and SEDs are overviewed..

Introduction

Vacuum microelectronics utilizing field emitter arrays (FEAs) have been showing tremendous progress and becomes attractive nanoelectronic technology for a new generation devices such as flat panel displays, ultrahigh-frequency devices, and so on [1-3]. However, there are important limitations of FEAs in their reliability and efficiency [3]. Transfer Mold fabrication method has been developed to fulfill the requirements of the emitter tip sharpening, the emitter material selection, uniformity and reproducibility. The tip sharpness of less than 10nm (2.5-5nm) radius, the good uniformity and the low work function material usage for FEAs, have been obtained [4-10]. The Transfer Mold fabrication technique has been one of the best technique of getting and controlling the nanometer level device structures as well as FEA structures. The technology of carbon nanotubes, nanocrystalline, and Surface Conduction electron Emitters(SCEs) have also advanced for vacuum nanotechnology.

In this paper, the Transfer Mold emitter fabrication technique is described for realizing high efficient and high reliable vacuum nanoelectronic devices, especially, vacuum microelectronic power switching devices, as well as large nanodevices [10]. The carbon nanotubes, Si nanocrystalline, SCEs and their application for FEDs are mentioned as well.

Transfer Mold Fabrication Technique

Transfer Mold fabrication process is illustrated in Fig. 1. First, (100) Si substrate is anisotropically etched through a thermally oxidized SiO_2 mask using 30% KOH aqueous solution to make pyramidal holes with very sharp corners, i.e., "Molds." On the contrary to the conventional fabrication method for Si FEAs using Si anisotropical etching, the etching process is automatically stopped. Thus, it is easy to make lots of molds uniformly and reproducibly. The widths of the openings usually range from 0.8 to 3.0μm. After removing SiO_2 mask, the Si molds are thermally oxidized to form emitter-to-gate high quality insulator layer with few leak. The resistivity of thermal oxidized SiO_2 layer is twice or three times as high as that of deposited SiO_2 insulators. During the thermal SiO_2 layer growth, the SiO_2 layer shapes on sidewalls of the molds have become convex. Subsequently, emitter materials are deposited on the SiO_2 layer by sputtering to fill the molds. The convex shapes of the Si molds sharpen the emitter tips at the bottom of the molds.

Then, the emitter material layer is bonded with a glass substrate having an Al rear surface electrode by applying DC several hundred voltages. Next, an anisotropic Si etching by tetramethyl ammonium hydroxide (TMAH) solution and a SiO_2 etching by buffered HF solution are used to remove the Si mold substrate and the SiO_2 Layer. The SiO_2 layer acts as an etching stop layer for TMAH solution. Thus, the emitter array is transferred from the Si substrate to the glass substrate. Since emitter tips are intrinsically sharpened in the process, there is no need to sharpen them after their formation [4-10].

In order to make gated emitter array, following process are needed. Gate layer and resist layer are coated on the SiO_2 layer, which is not removed in the gate fabrication process. The thin resist layer is dry etched in an oxygen plasma to reveal only the tips of the coated emitters. Finally, wet etchings of both the gate and the oxide result in submicron openings in the gate center on the emitters.

Figure 2 shows SEM micrograph of the gated Transfer Mold Mo FEAs. The emitter array has 10,000 emitter tips. Emitter base lengths are 1.6μm. The emitter tips are extremely sharpened to less than 10 nm radii, because of the sharpening effect on the tips by the Si mold surface oxidation. The I-V characteristics of the gated Transfer Mold Mo FEA at the pressure of 3.9×10^{-5} Pa is shown in Fig. 3. The emitter base length is 1.6μm. The distance between the emitters and the gates and that between the emitters and the anode is 0.4μm and 500μm, respectively. The voltage between the emitters and the anode is kept at 350V. The turn-on voltage is as low as 7 V without high vacuum baking, because the tips are extremely sharpened to less than 10nm radii by the usage of the sharpening effect during Si single crystal mold surface oxidation. Even if tip radii are sharpened and the electrode distance are so close each other, the extraction voltages of field emission need more than the surface barrier heights, that is, the Mo work function of 4.5eV. Therefore, the turn-on voltage of 7V is almost close to the theoretical value. Moreover, the voltage is less than the residual gas theoretical ionization voltages of 12 to 20V.

The Transfer Mold fabrication technique is useful for fabricating sharp, uniform, low operating and high integrated large area FEAs.

Carbon nanotube FEDs

The recent nanotechnology trend has been paying much attention to the carbon nanotubes (CNTs) as the promising nanomaterials, especially, the emitter materials [11,12]. CNTs are composed of graphite sheets rolled into seamless hollow cylinders with diameters ranging from 0.7nm to approximately 50nm, and their length are more than 10 m. The electron emission is observed at the end of nanotubes. The CNT characteristics of high aspect ratio and small tip radius are good advantage for field emitters.

Moreover, they might be capable of operating in low vacuum atmosphere because of chemically inactive and stable

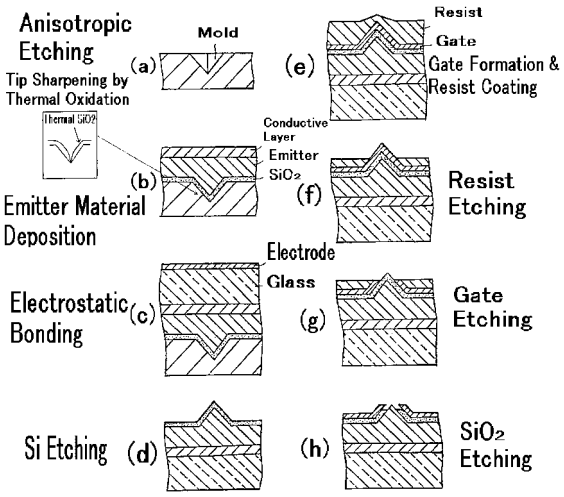

Figure 1 *Transfer Mold fabrication process*

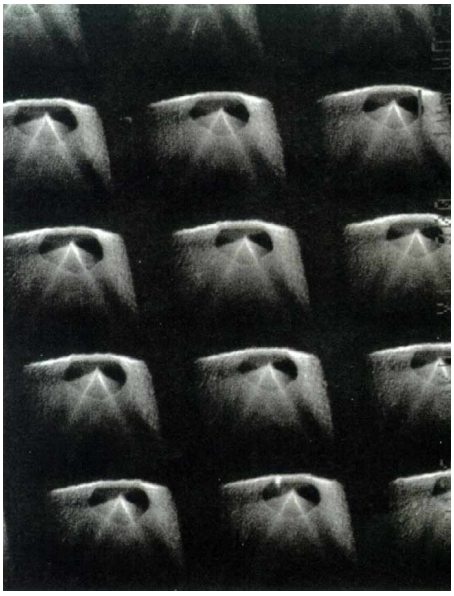

Figure 2 *SEM micrograph of the Gated Transfer Mold Mo FEA*

characteristics. Two types of CNTs, the multi-wall nanotubes (MWNTs) and the single-walled nanotubes (SWNTs), are classified by a number of their rolled seamless graphite sheets. CRT (cathode ray tube) type light source tube for FED element was reported in 1998[12]. MWNTs by arc discharge between graphite electrodes were used. First, MWNTs were directly glued onto a stainless steel plate by using conductive paste. Subsequently, the screen printing technique was used for industrial application. A grid electrode is used as an extracting electrode in the light source tube. The distance between the CNT cathode and the grid is 0.2-1.0mm. The grid voltage Vg, the phosphor anode voltage Va, and the emission current Ie are 300-500V, 10-12KV, and about 200 A, respectively. The luminance of the phosphor screen for ZnS:Cu,Al(green), Y_2O_3:Eu (red), and ZnS:Ag (blue) are $6.3x10^4$Cd/m2, $2.3x\ 10^4$Cd/m2, $1.5x\ 10^4$Cd/m2, respectively. The luminous efficiency was 70lm/W for green. The luminance and the luminous flux have been reached to $1x\ 10^6$Cd/m2 and 1000lm in high voltage acceleration of more than 35kV[15-16].

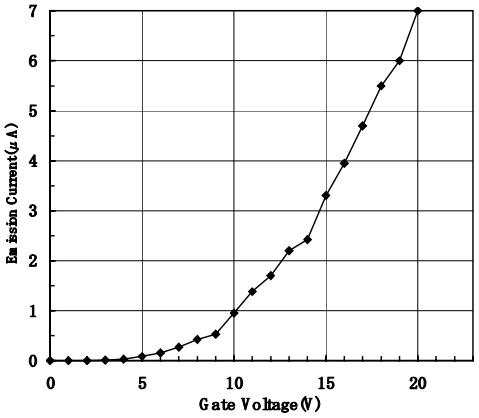

Figure 3 *I-V characteristics of the Gated Transfer Mold Mo FEAs*

Figure 4 *riode type 40-inch size CNT-FED*

Diode type and triode type FEDs were also developed in 1998, 1999, and 2002[12, 13, 17]. Figure 4 shows the photograph of the triode type 40-inch size CNT-FED. The outer size is 990x570x7mm. The screen size is 868.7x518.2mm. The pixel size and the pixel number are 2.54x7.62mm[3(RGB) x2.54mm] and 324x204[68RGB], respectively. The gate-insulator composite substrates are also used as the extracting electrodes in the triode FED. The CNTs is double-walled-nanotube (DWNT). A high voltage of typically 5kV is applied to the anode. The luminance of the green color is approximately $1.0x10^5$Cd/m2 under dc-driving.

Though CNT FEDs are one of the promising FEDS, the technology issues of non-uniformity emission, field evaporation, low cost CNT manufacturing method, large area CNT emitters, triode structure, and spacers should be solved.

Si nanocrystalline FEDs

Ballistic electron surface-emitting cold cathode based on nanocrystallized polysilicon (NPS) has been developed for FEDs

[18-21]. The electron emission mechanism from the NPS structure is due to a multiple tunneling effect proposed as quasi-ballistic electron transport. First, electrons are injected from the substrate due to thermal excitation. Because the electron drift length in silicon nanocrystallites is much longer than bulk silicon, the collision probability is considerably small. Major potential drop is produced in the PPS layer, especially in the region of near the PPS surface. The injected electrons are accelerated by the strong electric field of approximately 10^5V/cm and drifted through the NPS layer toward the surface electrode. The hot electrons are emitted into the vacuum through a thin Au film electrode. The NPS layers can be deposited on Si, quartz, and glass substrates. Figure 5 shows 2.6-inch size display using the ballistic electron surface-emitting cold cathode on a glass substrate. The nember of the pixels is 168(RGB) x126. The sub pixel size is 320x107μm. P22 phosphor screen is used as an anode and placed at a distance of 3mm from the cathodes. The anode voltage is 6kV. Though the emission efficiency is approximately 1.5%, the ballistic electron surface-emitting cold cathodes have the advantages of narrow electron emission trajectory, no focusing electrode, low operation voltage of 16V and low vacuum operation.

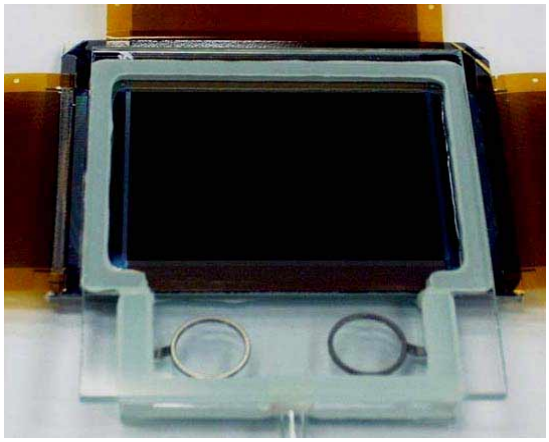

Figure 5 *2.6-inch size display using the ballistic electron surface-emitting cold cathode on a glass substrate*

Surface-conduction Electron-emitter Displays (SEDs)

36-inch surface-conduction electron-emitter displays (SEDs), consisting of surface conduction electron emitters (SCEs) and a phosphor screen for CRTs, have been developed by Toshiba-Canon Alliance [22]. The main features of the prototype are luminance of 400 cd/m2, contrast ratio of 100,000: 1 in a dark room, and response time of <1 ms.

The SED has a simple device structure as shown in Fig. 6, consisting of SCE cathodes on a glass plate and a high-voltage anode plate. Ink-jet printing is used to deposit a thin palladium oxide film on the cathode plate. Electron emission portions are formed by applying voltage to the thin palladium oxide film placed between two electrodes. The anode plate has a stripe-patterned phosphor screen with color filter layer covered with a metal backing film. The SCE cathode plate consists of a simple matrix-wire structure. The SED is driven by line sequential scanning,. The scanning circuit generates the scan signal, the amplitude of which is Vscan, and the signal modulation circuit generates a pulse width modulation signal which is synchronized with the scan signal.

A 36-inch diagonal SED prototype with 1280 (H)×3 (R/G/B)×768 (V) pixels has thin spacers, which allow the panel vacuum structure to be sustained under atmospheric pressure. Thin spacers are placed on the printed wires to avoid disturbing the electron paths. The cathode plate and anode plate are sealed by frit glass and a low melting point metal. The thickness of the panel was 7.3 mm, which is the sum of 2.8 mm (cathode plate), 2.8 mm (anode plate) and 1.7 mm (vacuum spacing). The panel weight is 7.8 kg. The anode plate has a stripe-patterned P-22 (R/G/B) phosphor screen with color filter layer covered with a metal backing film. The main features of the prototype panel such as luminance, contrast, response time have achieved sufficient performance for application to TV. The SED provides high image quality comparable to that of CRTs.

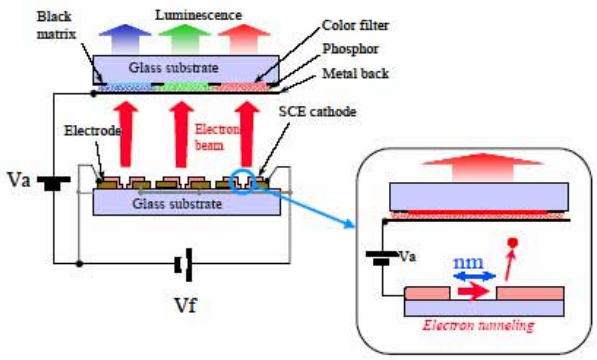

Figure 6. *SED Structure*

Conclusion

Vacuum microelectronics has been advancing toward vacuum nanotechnology with nanomachining and nanomaterials. The Transfer Mold technique has been applied in the fabrication of sharp, uniform, low operating and high integrated large area FEAs. The emitter tip radii are as low as less than 10nm(2.5-5nm). The emitter shapes exhibit high uniformity. The turn-on voltage of the Transfer Mold Mo FEAs is as low as 7 V without high vacuum baking. Transfer Mold technique is appropriate for fabricating sharp, uniform, low operating and high integrated large area FEAs as well as nanodevices. 40'' diagonal triode type CNT FED was developed. The luminance of the green color is approximately $1.0x10^5$Cd/m2 under dc-driving. Though the issues of non-uniformity emission, low cost CNTs, large area CNT emitters, triode structure, and spacers are remaining, the CNT FEDs as well as Ballistic electron surface-emitting cold cathode are one of the promising FEDs.

The SEDs providing high image quality comparable to that of CRTs are around the corner.

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Author Biography

Masayuki Nakamoto was born in Tokyo, Japan, in 1951. He received the B. S., M. S. from Yokohama National University, and Sc. D. degree from Tohoku University, respectively. He was a Visiting Professor at MIT(1986-1988) .He joined Toshiba Corporation in 1977 and has been a professor of Shizuoka University from 2004. Since joining Toshiba Corporation , he has been doing research on the rare-earth phosphors, the infrared sensors, the magneto-optical sensors, vacuum nanoelectronics, especially, FEDs and NEMS. He is a member of the program committee of the Society for Information Display..