Fixed Pattern Noise in Pixels with Combined Linear and Logarithmic Response

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Abstract

Linear pixels like CCD and CMOS APS, have a limited dynamic range of 2-3 decades, while wide dynamic range logarithmic pixels have reduced sensitivity at low light. Pixels, which integrate the photo-generated charge for low intensity and use a logarithmic load for high intensity, combine the better features of the two types of pixel. However, device mismatch between pixels and the linear-logarithmic response combine to create several sources of fixed pattern noise. In this paper, a device-physics based model of the pixel response is used to characterize these sources of fixed pattern noise and study their impact on the output image produced from pixels manufactured in a typical CMOS process.

Introduction

Wide dynamic range imaging has been an area of interest owing to the inability of popular sensors like CCD and CMOS based active pixel sensors to capture the high dynamic range of about 6-7 decades available in nature. Scenes with this wide dynamic range can be imaged using logarithmic pixels that compress the dynamic range of the input signal using the subthreshold region of operation of a transistor [1]. With proper calibration techniques to remove fixed pattern noise, these pixels are capable of producing images with a relative contrast threshold of 2%, and hence match the performance of human eye [2]. However, logarithmic pixels suffer from long settling time effects and sensitivity degradation at low light conditions, owing to the parasitic leakage current within each pixel [3]. To alleviate this problem, pixels have been manufactured which integrate the photocurrent on the diode capacitance for low illumination and use a subthreshold load to compress the high illumination intensities [3, 4, 5, 6, 7]. This results in a linear response for low intensities, and a logarithmic response for high intensities. For convenience, these pixels will be referred to as LLCMOS pixels.

In this paper, earlier works on the study of fixed pattern noise in logarithmic sensors [2] and modeling of LLCMOS pixels [8] are extended to the study the fixed pattern noise profile of LLCMOS pixels. In the next section, a brief summary of the operation of LLCMOS pixels will be presented. Experimental results from pixels manufactured in a typical 0.35μm process along with a model to explain the behavior of these pixels will also be presented. The presence of fixed pattern noise in LLCMOS pixels will be shown through the responses of four typical pixels. This will be followed by an explanation of various contributing elements to the fixed pattern noise. In order to study this noise, the model for pixel response will be combined with that of the readout chain to introduce a parametric model for the output from a pixel array. A simple parameter extraction strategy for the model parameters will also be described. The model will be used to characterise the fixed pattern noise in various regions of operation of LLCMOS pixels. In the penultimate section of the paper, the type of fixed pattern noise correction needed to produce good quality images from arrays of LLCMOS pixels will be described.

Pixels with Combined Linear and Logarithmic Response

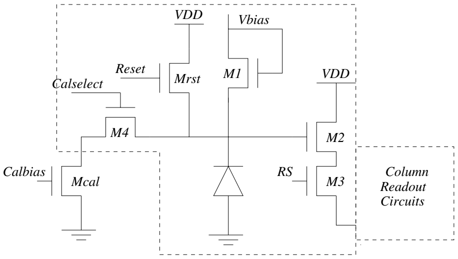

Figure 1. *Pixel with combined linear and logarithmic response*

Pixels have been proposed that combine the high dynamic range of logarithmic pixels with the low light sensitivity and speed of response of linear pixels, using a single frame readout [3, 6, 7]. The operation of these pixels can be understood with the aid of the schematic circuit diagram in Figure 1. With this pixel, the process of forming an image starts by resetting the photodiode node to a voltage that is higher than the bias voltage V_{bias} using the reset transistor. When this reset transistor is turned off at the beginning of an integration time, the capacitor connected to the photodiode is discharged by the photo-generated current flowing through the pixel. Initially, this leads to a linear relationship between the node voltage and the photocurrent. However, if the capacitor is discharged for long enough, the voltage on the photodiode node will bias transistor $M1$ into weak inversion. Once this occurs, some of the photocurrent will flow through transistor $M1$. If the integration time is long enough, all the photocurrent will eventually flow through $M1$. When this occurs the node voltage will reach a steady state value that represents the logarithm of the photocurrent. If the node voltage is sampled after a constant integration time, the result is a pixel with a linear response at low photocurrents and a logarithmic response at higher photocurrents. Within a camera, this voltage output of the pixel is typically sampled using the selectable source-follower formed by transistors $M2$ and $M3$ to create a voltage on the shared output line that is proportional to the voltage within the pixel. It may be observed that the transition point between the linear and logarithmic region of responses of LLCMOS pixels can be modified by changing either the bias voltage V_{bias} or the integration time.

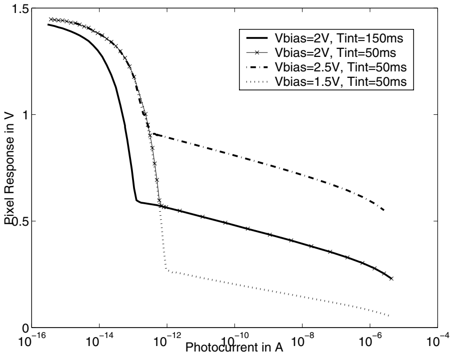

Figure 2. *Experimental response curves from the pixel showing the pixel's output at various photocurrents and at various bias voltages and integration times*

Figure 2 shows the measured response of LLCMOS pixel at different bias voltages, V_{bias}, and integration times, t_{int}. The pixel had dimensions of 10μm$\times 10\mu$m with a fill factor of 44% and it was manufactured in a typical $0.35\mu m$ CMOS process from Austria Microsystems. These results show the expected transition from a linear response at small photocurrents to a logarithmic response at higher photocurrents. In addition, the different sets of data show that, as expected the photocurrent, at which the transition between the two types of response occurs, decreases when either the integration time or the bias voltage increases. To explain the unique behavior of the circuit, we have proposed a model based on the device physics of the transistors used [8]

$$\begin{aligned} V_{out} &= n\phi_t \log \left[\exp\left(\frac{V_{reset} - t_{int}(I_{ph}+I_{dark})/C}{n\phi_t} \right) \right. \\ &+ \left. \frac{\left(1-\exp(-t_{int}I_{ph}/n\phi_t C)\right) R_0}{I_{ph}} \right] \end{aligned} \tag{1}$$

where I_{ph} is the photocurrent, I_{dark} is the leakage current which flows through the photodiode in absence of any input illumination, t_{int} is the integration time and the parameter $R_0 = 2I_0 e^{(V_{bias}-V_{T,M1})/n\phi_t}$ has been included for convenience. V_T is the threshold voltage of the transistor concerned and I_0 is the In addition to the reset voltage, the response of the imager can be explained by the four parameters C, I_{dark}, $n\phi_t$ and R. At low photocurrents or for a short integration time, the first part of the argument of the logarithm of Equation 1 dominates and this equation reduces to the simple linear form

$$V_{out} = V_{reset} - t_{int}(I_{ph}+I_{dark})/C \tag{2}$$

Alternatively, at high photocurrents or after a long integration period, the second part of the argument dominates and Equation 1 reduces to the form

$$V_{out} = V_{bias} - V_T - n\phi_t \log(I_{ph}/2I_0) \tag{3}$$

which is equivalent to the model for the response of a logarithmic pixel developed by Joseph and Collins [1], when dark currents are negligible. This assumption is justifiable in the logarithmic region of the response of the LLCMOS pixel, because when I_{dark} is significant, the pixel operates in its linear mode. The transition region between the two, can be shifted by either changing the integration time or the bias voltage V_{bias}on the logarithmic transistor, $M1$. It can be observed that the model provides for linear response at low photocurrent or low integration time, and for a logarithmic response at high photocurrent or integration time. Further, the model also incorporates a quick but smooth transition between linear and logarithmic regions of operation, using parameters which can be obtained from linear and logarithmic regions of operations.

Fixed Pattern Noise

As is the common practice in pixel design, the photodiode area of the pixel was maximised to enhance the photon capture area of the pixel. This, added with the design constraint of having as small pixel as possible, to increase the resolution of the sensor meant that the transistors inside the pixel had to be designed using the minimum geometries possible. Minimum geometry transistor are susceptible to mismatch owing to process variations, resulting in the presence of fixed pattern noise in the images produced by the pixel array. This noise manifests itself as granular nature in the imager output when illuminated with an uniform scene. This noise is one of the most prominent limitations of the logarithmic pixels, and has been studied extensively in earlier works [1, 2].

To study the fixed pattern noise profile of LLCMOS sensors, experiments were performed with a 100×10 array of these pixels with a single stage readout. The array was tested using either a uniform light source produced by a 100 W, 12 V dc powered incandescent light source and integrating sphere assembly or a MOSFET acting as a voltage controlled current source [2]. The electronic current source, similar to the one used for calibration of logarithmic sensors [2] was added in every column of the array, as shown in Figure 1. The transistor $M4$ is used to select a particular row of pixels to be excited by the uniform current, while M_{cal} is the current source resident at the end of every column, that generates uniform currents for all pixels in the column.

Responses of 4 typical pixels from the array, to uniform illuminations has been shown in Figure 3. The response variation among the pixels is evident. In the linear region the voltage output of the array at uniform illumination had a range of 48mV . Considering the gain of the pixel in the linear region is approximately $1V/pA$ for the 50msec integration period, this would result in a noise of 50fA. Even at the highest photocurrent in linear region at around 1 pA, this contributes to about 5% contrast change. Similarly, the voltage output in the logarithmic region had a spread of 56mV around the mean output. The gain in the logarithmic region is of the order of 50 mV/decade and hence the fixed pattern noise of this amplitude will give an error of about a decade or 100% contrast change. This is even more serious than the linear region. Further, the transition point between the linear region to logarithmic region varies from pixels to pixels, by as much as fifth of a decade.

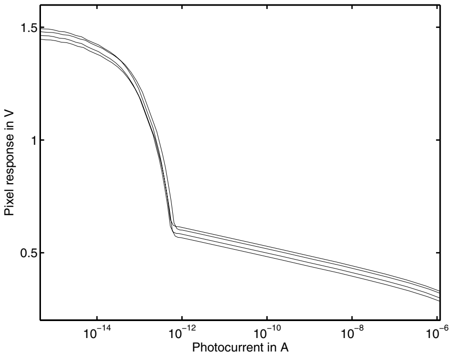

Figure 3. *Response curves of four pixels under uniform illumination with integration time of 50mSec and* V_{bias} *of 2 V*

Sources of Fixed Pattern Noise

The principal contributor to fixed pattern noise is the threshold voltage, V_T, variation in small geometry devices. In the LL-CMOS pixel, it affects the performance in all region of operations. V_{reset}, the voltage to which a pixel is reset using the transistor M_{rst} is approximately equal to $V_{DD} - V_{T,M_{rst}}$. Further, the output of the pixel during the logarithmic region depends on the threshold voltage of device $M1$ and the subthreshold slope variation of the same device, also forms a source of fixed pattern noise.

In addition to the pixel, various elements of the readout circuits also introduce fixed pattern noise. Prominent among these is the nMOS source follower device $M2$, which introduces a voltage drop in the readout path. This drop is dependent on the threshold voltage of $M2$, thereby introducing another source of fixed pattern noise. The source follower gain variation from pixel to pixel affects the output also produces fixed pattern noise in the pixel's output.

In the circuit schematic of Figure 1, only one addressing switch for the pixel is shown. However, in a two dimensional array, one needs two addressing mechanism to locate a pixel. To be able to do so, a second stage of readout circuits is added at the end of every column. In a conventional design the second stage is designed from pMOS transistors to compensate for the nMOS source follower loss in the pixel. In an alternate design, one may use differential amplifier readout circuits to provide high gain [2]. In either of the cases, a new source of column to column fixed pattern noise is introduced.

FPN Modelling

In order to characterise the fixed pattern noise in the pixel, we shall use the model used to study the pixel response [8], along with the effects of the readout circuits. The readout stages add an offset and provide a gain in the output. The response of a pixel in an array can hence be modelled as

$$V_{out,array} = O_{readout} + G_{readout} * V_{out,pixel} \tag{4}$$

where $O_{readout}$ is the net offset in the readout chain and $G_{readout}$ is the total gain in the readout chain. Combining equation 1 and 4, we may write a combined parametric expression of the output of the pixel as

$$\begin{aligned} y \;=\; & P\log\left[\exp\left(\frac{V_{reset,out} - t_{int}(I_{ph}+I_{dark})Q}{P}\right) + \right. \\ & \left. \frac{\left(1-\exp(-t_{int}I_{ph}Q/P)\right)R}{I_{ph}}\right] \end{aligned} \tag{5}$$

where

$$V_{reset,out} = G_{readout} * V_{reset} + O_{readout} \tag{6}$$

$$P = G_{readout} * n\phi_t \tag{7}$$

$$Q = G_{readout} * \frac{1}{C} \tag{8}$$

$$R = R_0 * \exp\left(\frac{O_{readout}}{G_{readout}}\right) \tag{9}$$

The final form of the response as shown in equation 5 is very similar to that of pixel response model of equation 1 and hence can be broken in two simple equation in a way similar to that of equation 1. The output in the linear region can be given as

$$V_{out,array,lin} = V_{reset,out} - t_{int}(I_{ph}+I_{dark})Q \tag{10}$$

The contributors to the fixed pattern noise according to the model, in the linear region are the V_{reset}, offset and the gain of the readout chain. It may be observed that any variation in $V_{reset,out}$ appears as an offset variation in the output in linear regions, while Q affects the gain variation of the output in linear region. It is a general practice in linear active pixel sensors to record the value of $V_{reset,out}$ along with the pixel output, to remove all offset variations. Hence, $V_{reset,out}$ will not be referred as a parameter of the pixel response.

Variations in P, and hence the subthreshold slope, $n\phi_t$, of the logarithmic load device along with the gain of the readout, affects the gain in the logarithmic region. P along with R, and hence the offset of the readout along with threshold voltage variation of the logarithmic load device, affects the offset in the logarithmic region, as the output in the logarithmic region is given by

$$V_{out,array,log} = P\log R + P\log(I_{PH}) \tag{11}$$

Equations 10 and 11 enable a four-measurements scheme to extract the parameters to completely characterise the pixel. Two measurements in linear region are needed, one at a typical illumination to extract Q, while another at the dark response to extract I_{dark}. Similarly, in the logarithmic region, two measurements can be used to extract P and R, in a way similar to that for conventional logarithmic pixels [2]. The extracted parameter of an array of the pixels can be used to study the fixed pattern noise profile of the imager.

Equally important is the fact that the model predicts the transition region and hence the shift in the transition regions of the image sensor, without explicitly incorporating a different parameter. Thus, the variation in the transition region from pixel to pixel can be predicted using the parameters from linear and logarithmic region of operation.

Experimental Studies of Fixed Pattern noise

The model described in the previous section was used to extract the parameters of pixels from a 100×10 array, described in the second section of the paper. The statistical values of various model parameters are described in the table. The principal nature of the fixed pattern noise in both regions of operation is that of an additive offset. In the linear region, variations in $V_{reset,out}$ contributes to the offset FPN and can be corrected by recording its value with the output of the pixel. A good quality image in the linear region can be obtained by offset only correction. This situation arises because the 0.5% gain variations results in a relative error in the output of the offset corrected image in the linear region of the order of 0.5%. This is smaller than the contrast limit of human visual system which is in the range of 1-2% [9].

Model	Parameter	Mean	Standard Deviation
P	(mV/decade)	53.6	0.31
Q	(mV/mSec-fA)	12.1	0.065
R		17.73	9.5
I_{dark}	(fA)	0.81	0.44

Statistical variation of the different model parameters

Since the sources of offset variations are different in the two regions of operation, this fixed pattern noise correction scheme does not correct all of the offset variations in the logarithmic region. A seperate offset correction is therefore required in this operating region. In the logarithmic region, an offset only correction scheme [10] will have a residual error of

$$\Delta V_{out} = \Delta P \log(I_{ph}/I_{corr}) \tag{12}$$

where I_{corr} is a typical current used in subtractive offset correction. The equivalent percentage error in apparent contrast of the residual image, K, of this pixel would be given by

$$K = \frac{\Delta P}{P} \log(I_{ph}/I_{corr}) \tag{13}$$

Since the logarithmic region extends to about 5 decades in typical operation of LLCMOS pixels, the offset corrected image can meet the performance of human eye only if the gain variation is of the order of 0.08%. Since this level of variations has not been achieved by the pixel array, gain as well offset correction is needed in the logarithmic region to produce high quality images.

Conclusion

Pixels with combined linear and logarithmic response (LLCMOS) have a dynamic range of 9 decades, without the problems of low light sensitivity degradation and long settling time effects, often associated with logarithmic pixels. Further, the additional gain obtained in low light regions improves the image quality in darker regions of typical world scenes. However, owing to the unique response they have, the fixed pattern noise profile of an array of such a sensors is different from that of linear or logarithmic pixels.

In this paper, a model based on the device physics of the transistors used in the pixels as well as the readout circuits, is used to explain the fixed pattern noise behavior of LLCMOS pixels. Experimental results from a typical array have been presented. Based on the statistical values of various parameters obtained from these experiments, it has been proved that offset only correction should be sufficient for a good quality image in the linear region of operation of such imagers. However, in the logarithmic region of the operation of the LLCMOS pixels, one needs to correct for offset as well as gain to produce contrast properties comparable to that of human visual system. Future work will concentrate on devising a fixed pattern noise correction strategy based on the model and a study of column to column fixed pattern noise in large arrays of LLCMOS pixels.

References

[1] D.Joseph and S. Collins. “Modelling, calibration and correction of illumination-dependent fixed pattern noise in logarithmic CMOS image sensor” In *IEEE Trans. Inst. and Meas.*, 51(5), October 2001.

[2] B. Choubey, S. Aoyoma, S. Otim, D. Joseph, and S. Collins, “An electronic calibration scheme for logarithmic CMOS image sensors,” *accepted for IEEE J. Sens.*, 2005.

[3] B. Choubey, and S.Collins, “A reduced leakage current wide dynamic range CMOS pixel” In *IEEE International Midwest Symposium on Circuits and Systems, 2005, Cincinnati, USA*

[4] Dalsa.Inc. *1M75-SA Stop-Action Camera*

[5] Photon Focus *http://www.photonfocus.com/*

[6] Eric C. Fox, Jerry Hynecek, Douglas R. Dykaar “Wide-dynamic-range pixel with combined linear and loogarithmic response and increased signal swing” *Presented at the IS&T/SPIE 12th International Symposium on Electronic Imaging 2000*, January 23 to 28, 2000.

[7] W. Martin, “Optoelectronic sensor,” European Patent 03/032394 A1, April 2003.

[8] B. Choubey, and S.Collins, “Device physics based model for pixels with combined linear and logarithmic response” *submitted for publication*

[9] B. Wandell, *Foundations of Vision.* Sinauer Associates, 1995.

[10] S. Kavadias, B. Dierickx, D. Scheffer, A. Alaerts, D. Uwaerts, and J. Bogaerts, “A logarithmic response CMOS image sensor with on-chip calibration,” *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1146–52, August 2000.

Author Biography

Bhaskar Choubey received his B.Tech. from Regional Engineering College(now NIT), Warangal, with a Gold Medal for best outgoing student. He was awarded the Rhodes scholarship in 2002 to persue higher studies in University of Oxford, where he is working towards his doctorate in the field of wide dynamic range CMOS imagers. In 2005, he was a visiting scientist at Max Planck Institute of Brain Research, working on visual psychophysics.

Steve Collins received a B.Sc. in Theoretical Physics from the University of York in 1982 and a Ph.D. from the University of Warwick in 1986. From 1985 until 1997 he worked at the Defense Research Agency on various topics including the origins of 1/f noise in MOSFETs, image sensors and analogue information processing. From 1997 he has been at the University of Oxford were he has continued his interest in smart imaging sensors and non-volatile analogue memories.