# The 3D Multiplexer Data Registration Architecture For High Performance Inkjet Printhead

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## Abstract

*This novel three dimensional data registration scheme is employed to reduce the signal scanning time to 30% compared to that of the conventional 2D architectures. Large array (>1000) format inkjet printhead will be the major applicaton. The three dimensional have the relationship of* $X=3\times\sqrt[3]{Y}+1$ *(X~Data Connection lines Y~Nozzles) , To simultaneously write the signal into the 3D driving circuit .Resulting in 5 pads required for controlling 400 nozzles by de-multiplexer circuit .The desired signal for S selections and A selections can be pre-registered and latched in the circuit for one time writing. This technology could be applied not only on the inkjet printhead products but also on many other applications.The smart printhead has been designed by a 0.35 um CMOS processes. The physical design rules of 0.35um 2P2M 5V, (Double Poly Double Metal) MIXED-MODE processes. This study develops the integrated multiplexer driver inkjet head (IMDH) by a standard CMOS processes to reduce the connecting addresses needed and enhance high speed printing for controlling the nozzle orifices which ejection the small size of droplet. We have fabricated a printhead driver chip controlled beyond 400 nozzles with a 5 pl. ink drop volume .*

## Introduction

One of the major goals for advanced inkjet printhead design is to optimize printing quality and speed while minimize cost. To achieve this, large array inkjet nozzles would be desired but the total chip area need to be maintained, thus resulting in the reduction of the area of driving circuit [1][2]. In the past 20 years, inkjet printheads have been extended in the nozzle numbers from tens to hundreds in the recent years and further to thousands in the future, while intending to maintain data accessing points in the order of 20-40. To achieve this, the most commonly employed architecture of driving IC for commercial inkjet printhead nowadays is carried out by two-dimensional arrayed-switches. The data accessing points will be N(Pads) $=2\times\sqrt[2]{Y}+1$ (Y~Nozzles), which is equal to 21 if the nozzle number is 100. However, if the nozzle number increases to thousands in a large array format injet printhead, not only the data accessing points will be easily increased to hundreds, but also the scanning time will significantly rise, which deteriorates the performance of inkjet printing.

In this study, a three dimensional data registration scheme to reduce the number of data accessing points as well as scanning lines for large array inkjet printhead with nozzle number more than 1000 is proposed. The total numbers of data accessing points will be $N=3\times\sqrt[3]{Y}+1$, which is 31 for 1000 nozzles by the 3D novel design, a dramatic reduction from 68 if operated by the traditional 2D scheme. The enhancement will be even sounder in larger nozzle arrays. The scanning time is reduced up to 30% (The scanning speed is also increased by 3 times) thanks to the great reduction of lines for 3D scanning, in stead of 2D scanning.

The property comparison among 1D, 2D, and 3D architectures is listed in Table 1. As the nozzle number increases, a higher order circuit can effectively reduce the pad number.

**Table 1: Property comparison among 1D, 2D, and 3D driving schemes.**

| **X:Pads、Y:Nozzles** | X=Y+1 | $x=2\times\sqrt{Y}+1$ | $x=3\times\sqrt[3]{\sqrt{Y}}+1$ **(X:Connection lines,Y:Nozzles)** |
|---|---|---|---|
| **Nozzles** | 1000 | 1000 | 1000 |
| **Heaters** | 1000 | 1000 | 1000 |
| **Resolution (dpi)** | 300 | 300~600 | >600 |
| **Print Swath(in)** | 1/6 | 1/3 | >1/3 |
| **Interconnect Pad** | 1001 | 65 | 31 |
| **Scanning time** | 1msec | 90μsec | 30μsec |

## Circuit design,simulation,and characterization

Several options were considered for a conventional two-dimensional addressing circuitry. The three most promising were row-column demultiplexing (demux), blocking diodes, and a proprietary passive enhanced multiplexing scheme. The row-column scheme was chosen . This scheme reduces the number of pads from N(Pads) $=2\times\sqrt[2]{Y}+1$ for a printhead with Y resistors. When the row and column connected with the resistor cell are applied a positive voltage, the transistor will conduct and generate a current flow through the resistor . Then the resistor will heat the ink, generating bubbles to spray the ink droplets.

In the proposed novel 3D design, different from the 2D one, the control circuit is divided into two parts: the pass-gate device

(for signal path) and the power device (for power path), as shown in Figure 1.

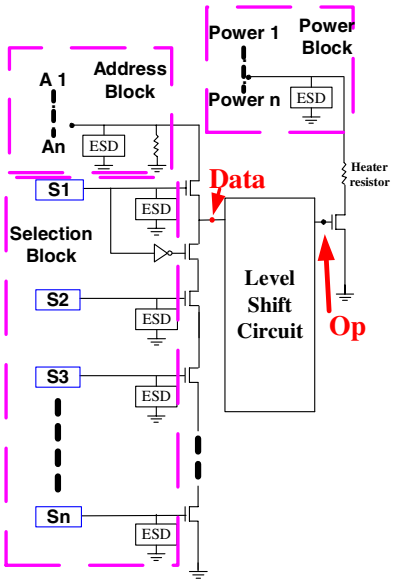


***Figure 1.*** *Three-dimensional printhead driving scheme*

The pass gate device is controlled by A selection and S selection, while the power line is controlled by P selection. To activate one heater, all P, A, and S selections are required to turn on at once. For example, to turn on the heater 1, $P_1$, $A_1$ and $S_1$ need to be set to high at the same time. Figure 2 illustrates the transient simulation of the input and output signal of the level shift device[3][4][5].

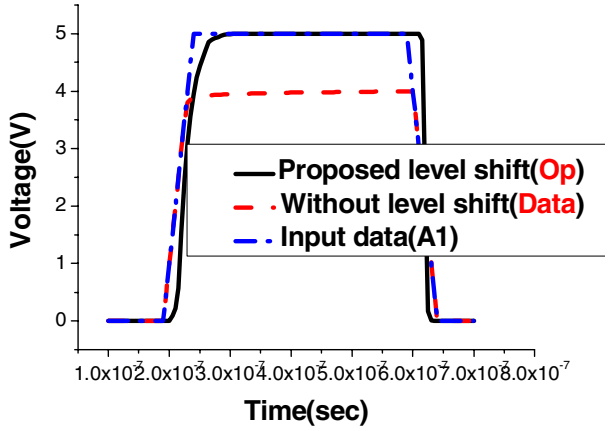


***Figure 2.*** *Transient simulation of the input and output signals of the level shift device*

The signal demonstrates not only the switch speed is higher by the level shift device than that of one without level shift circuit , but also the voltage has been enhanced to 5V [6][7][8]. Figure 3. shows the numbers of required connection pads for 1D, 2D and 3D control circuit.

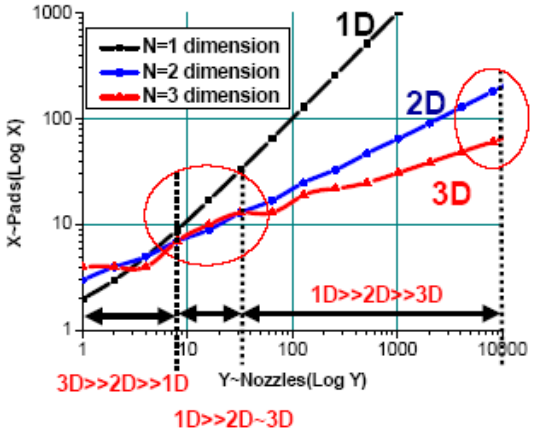


***Figure 3.*** *Connection Pads and Nozzles relationship*

As the nozzle number increases, the required connection pads are increasing but with different rates. The 1D case increase most rapidly while the 3D one increases slowest. There are two important intersections in the three curves, with the first one in the nozzle number of 10 and the second one in 30. When the nozzle number is much larger than 100, the 3D architecture can dramatically reduce the pad number in tens.

In turns of scanning rate, 3D architecture can be faster than the 2D one. For example, to drive125 nozzles, 2D structure may employ 8 primitive and 16 address selections. The scanning time from the first address line to the 16th is shown in Figure 4a, will take 16 clock time. However, in the 3D structure, only 5 clock time will be taken for driving the last nozzle as shown in Figure 4b, thus the time will be reduced to 30% in maximum. On the other hand, the total connection pads for the 2D and 3D circuit structure in this case are 25 and 16 (including one for common line), respectively, demonstrating fewer pads needed in the 3D design

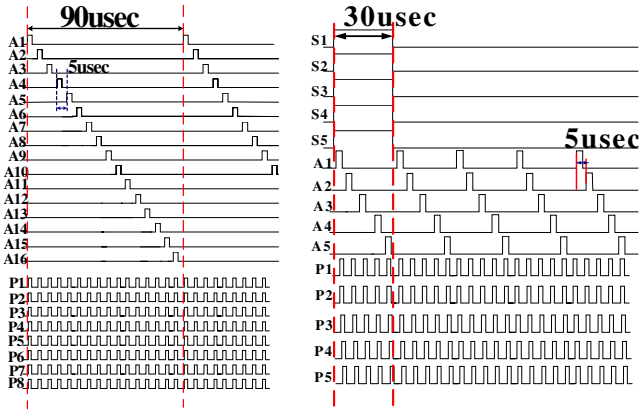


***Figure 4.*** *The sequence of driving signals for (A) 2D method and (B) 3D method*

To simultaneously write the signal into the driving circuit, a de-multiplexer data latches and shift registers can be employed. The desired signal for S selections and A selections can be pre-registered and latched in the circuit for one time writing. Combining this scheme with the P selection control, simultaneous 3D driving can be realized.

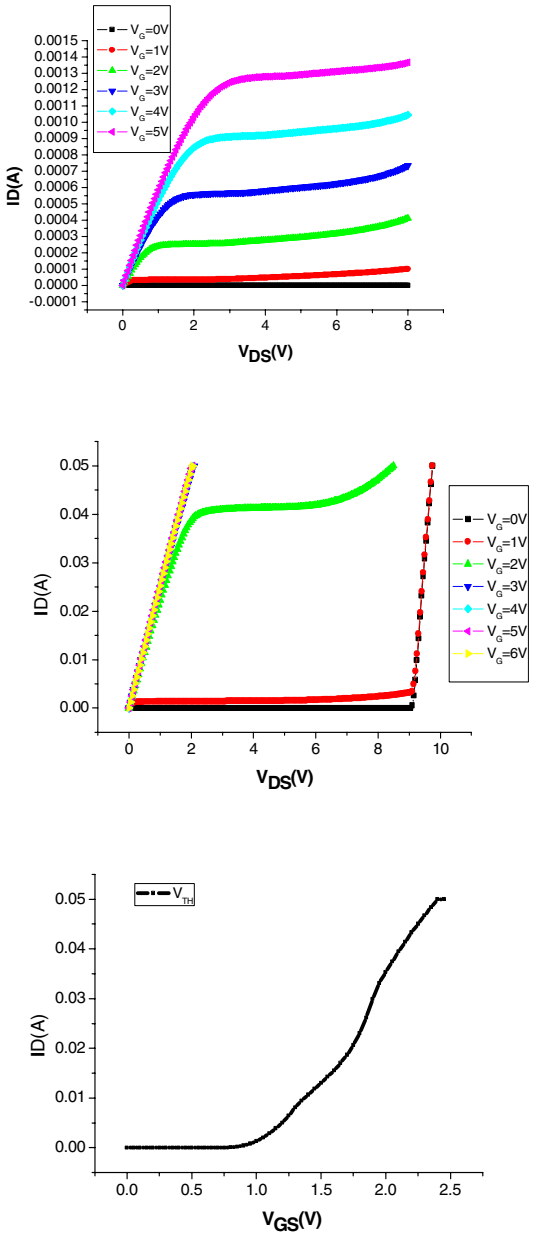


***Figure 5.*** *The pass-gate and CMOS driver characterist*

The characteristic of pass-gate device with 0.35 µm CMOS technology measured by HP 4156 semiconductor parameter analysiser is shown in Figure 5, showing that the break-down voltage close to 9 volts, higher enough for A selection signal passing through, and illustrating a driver functional circuit with a break-down voltage of 9 volts and gate threshold voltage of 1 volt , respectively. The signals for sequential nozzle driving and the measured result is shown in Figure 6, the probe point N1N97 on behalf of a signal (S1、A1、P1) passing through the D5,5 cell, and N5N204 represented 2D signal(A5, P5) controlling D5,5. The measured results verify the scan of the signal by 3D architecture is 34.4µs, faster than that by the 2D architecture with similar nozzle number.

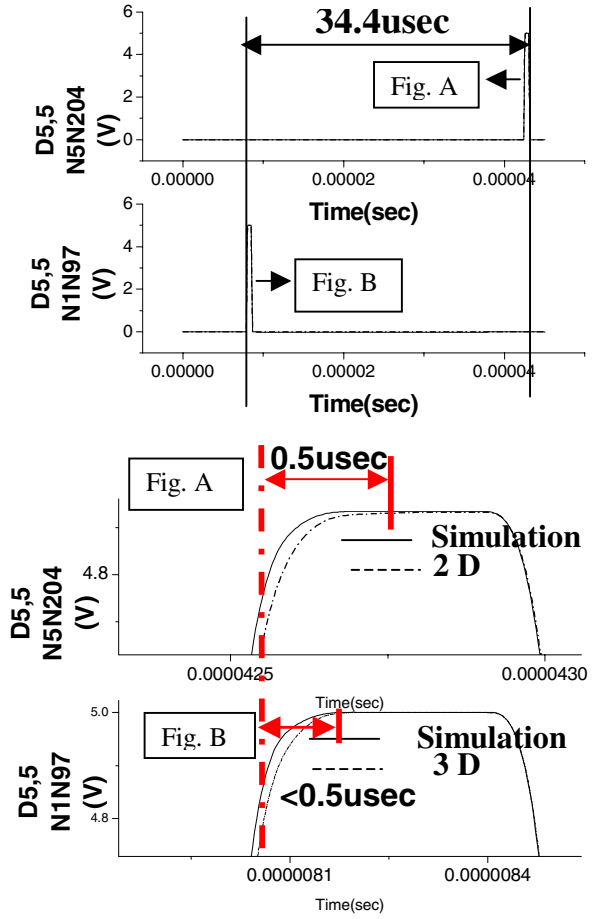


***Figure 6.*** *The signals for sequential nozzle driving and the measured result*

Figure 7. shows a photograph of the realized prototype. The area is 2.5 ×2.5 mm . Much care must be taken in the layout of the metal layers in order to avoid electromigration. The technology used was a two-poly four-metal (2P4M) 0.35um twinwell CMOS technology. This permits the connection of the bulk of every transistor to its source in order to avoid large gate–bulk voltages. A disadvantage of this principle is that it results in substrate currents near each NMOS transistor. Since the substrate is high-ohmic,

special attention went to the prevention of latch-up. Every transistor is surrounded by a full guard ring to make a good well contact.

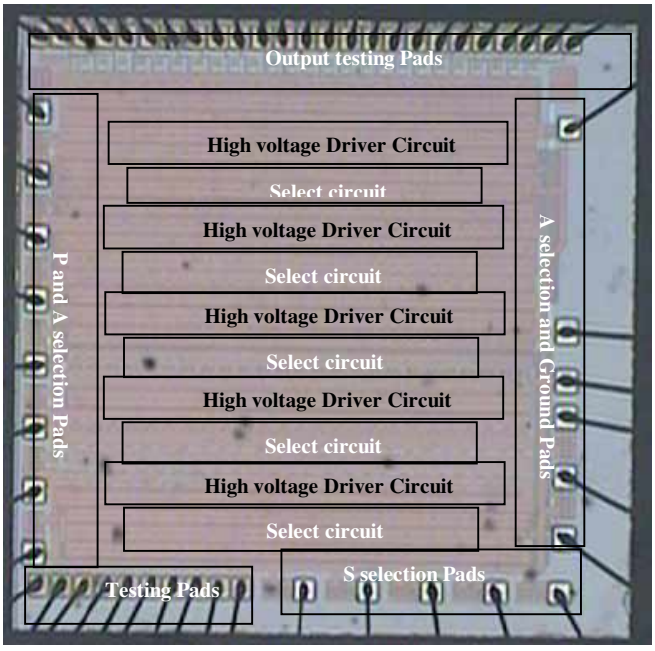


***Figure 7.*** *A photograph of the realized prototype.*

**Conclusions and future works**

This paper proposed a novel architecture of high-selection-speed 3D data registration for inkjet application specific integrated circuit (ASIC). The 3D driving architecture has successfully reduced the total numbers of control pads as well as scanning time up to 30%. This circuit has been designed, fabricated, and characterized, and demonstrate not only it's functionality but also the consistence between simulation and experiment results.

## Acknowledgments

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## References

[1]J. Stephen Aden, Jaime H. Bohórquez, Douglas M. Collins, M. Douglas Crook, André García,
and Ulrich E. Hess, "The Third-Generation HP Thermal InkJet Printhead", Hewlett-Packard Journal. pp.41-45 February 1994.

[2]Hue P. Le*,Le Technologies, Inc., Beaverton, Oregon, "Progress and Trends in Ink-jet Printing Technology, Part 2",Journal of Imaging Science and Technology ·VOL. 42, Number 1, pp.49–62 January/February 1998

[3]Bert Serneels,Tim Piessens,Michiel Steyaert, and Wim Dehaene, "A High-Voltage Output Driver in a 2.5-V 0.25-um CMOS Technology", IEEE JOURNAL OF SOLID-STATE CIRCUIT ,VOL. 40,NO.3,pp. 576 -583,MARCH 2005 .

[4] M. J. M. Pelgrom and E. C. Dijkmans, "A 3/5 V compatible I/O buffer,"IEEE J. Solid-State Circuits, vol. 30, no. 7, pp. 823–825, Jul. 1995.

[5] G. Singh, "A high speed 3.3 V IO buffer with 1.9 V tolerant CMOS process," in Proc. Eur. Solid-State Circuits Conf., 1998, pp. 128–131.

[6] H. Sanchez, J. Siegel, C. Nicoletta, J. Alvarez, J. Nissen, and G. Gerosa, "A versatile 3.3 V/2.5 V/1.8 V CMOS I/O driver built in a 0.2 um 3.5 nm tox 1.8 V CMOS technology," in IEEE ISSCC Dig. Tech. Papers, 1999, pp. 276–277.

[7] A.-J. Annema, G. Geelen, and P. de Jong, "5.5 V I/O in a 2.5 V in a 0.25um CMOS technology," IEEE J. Solid-State Circuits, vol. 36, no. 3, pp.528–538, Mar. 2001.

[8] B. Serneels, T. Piessens, M. Steyaert, andW. Dehaene, "A high-voltage output driver in a standard 2.5 V 0.25 _m CMOS technology," in IEEE ISSCC Dig. Tech. Papers, 2004, pp. 146–147.

## Author Biography

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