Parallel Signal Processing System for a Super High-Resolution Digital Camera

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Abstract

The technology of the digital still camera has recently achieved remarkable progress. The number of pixels in the main stream of consumer-use cameras has reached the 3 million-range, with 5 million the maximum. And for professional-use, the number of pixels has reached the 16 million. Digital still cameras convert signal data generated from these pixel CCD's to luminosity signals and chromaticity signals, which are compressed in conformity with JPEG standards by a signal processing circuit incorporated in the cameras.

The increase in the number of pixels results in the increase in the volume of signal processing, as a matter of course. In order to prevent increase in the recording time required for the increased volume of signal processing, the signal processing circuit has been designed and developed to process the signal at a higher rate, with the application of cutting-edge fine-fabrication technology of semiconductors. However, fine-fabrication with a design rule smaller than 0.09 micron needs a vast amount of investment for production, which might lead to a delay in the progress of high-rate processing. Therefore, a new technique of high-rate processing is required that does not depend on smaller scale fine-fabrication.

In this paper, we propose a technique for achieving the required high-rate signal processing by the use of parallel connection of the signal processing circuits necessary for handling signals of the digital cameras of high pixel-number CCD's. At the same time, we also report the excellent results obtained with a prototype camera made in accordance with our proposal.

1. Introduction

In the past few years, the market for the digital still cameras has been rapidly expanding. Since the introduction of a 1 M (million) pixel model in 1998 (1-3) and number of pixels has increased yearly from 2 M through 3 M up to 5 million.

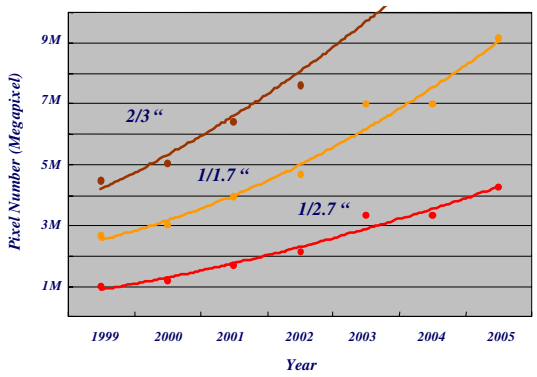

Figure 1. Yearly changes in number of pixels in marketed digital cameras

The increase in number of pixels has been realized by the progress in the fine-fabrication technology of semiconductors and that in the CCD-fabrication process. The processing rate of the signal-processing LSI has been accordingly increasing with the stepwise application of 0.35, 0.25, 0.18, and 0.13 micron rule technologies year after year. However, the fine-fabrication line beyond 0.09 micron rule requires a drastic hike in the investment for the semiconductor process, which may result in slower development of more advanced fine-fabrication.

In view of this situation, we propose a new technique, parallel processing, for calculation of luminosity, chromaticity, for JPEG processing needed for a digital camera installed with a high pixel CCD.

We have prepared a prototype camera based on the proposed technique, and the results of the prototype are reported as well.

1.1 Digital Camera System

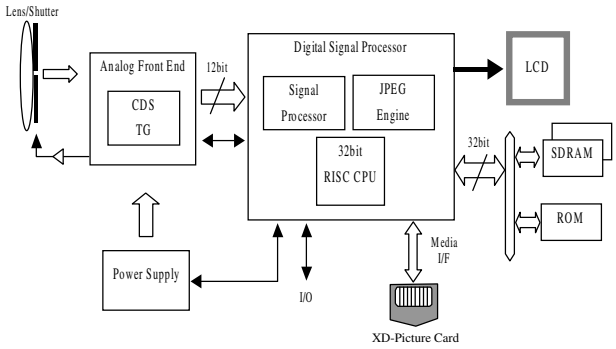

Figure 2. Digital camera system

Figure 2 shows the digital camera system. The major functions of this system, recording and reproduction, are explained as follows:

◊ ***Recording***

1. Signal generated from CCD converted digital signal by A/D convertor.
2. The CCD data is converted to luminosity data and chromaticity data.
3. The luminosity and chromaticity data are compressed with JPEG format.
4. The Data compressed with JPEG format is read out from the medium.

◊ ***Reproduction***

1. Data compressed with JPEG format is read out of the medium.
2. The JPEG-compressed data is expanded to produce luminosity and chromaticity data, and output to a monitor screen.

2. Parallel Processing Technique

The parallel processing technique is classified into the following two categories:

- Paralleled algorithms
- Parallel execution of algorithms

Our proposal belongs to the latter one.

2.1 Parallel Signal Processing

An effective technique of reducing the total processing time under a constant processing rate is to reduce the size of processing units. Application of this technique to the signal processing circuit means a greater number of processes executed in parallel that utilize pixels in peripheral areas such as digital filters. This situation may generate increase in the mutual dependence of data among the simply divided pixels, or data exchange among the parallel processing units, which may reduce the intended speed-up effect. As is shown in Fig. 3, however, this problem will be overcome by the overlapped use of the filter-delay elements of the signal processing, which allows independent execution of each processing unit, and allows reduction of the total processing time in proportion to the number of portions which are parallel-processed.

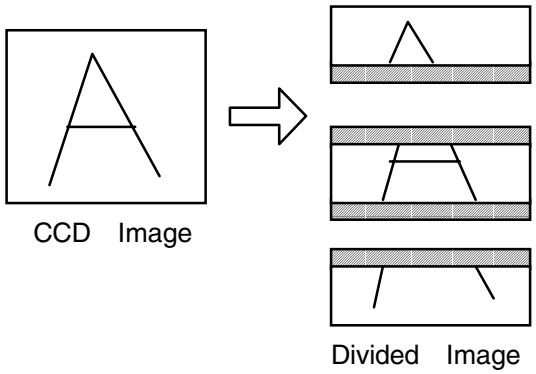

Figure 3. Parallel signal processing

2.2 Parallel Processing of JPEG Compression

As in the case of the signal processing described above, the total time for JPEG compression processing can be reduced by educing the size of processing units. In the case of JPEG compression, however, the compressed data is of variable length depending on the relevant image, and moreover, it is embedded with a control code called a restart marker at periodic intervals corresponding to the original image. As a consequence, a simple combination of the divided JPEG-compressed images will not always have the periodicity of the restart markers which are required, and thus it is not consistent with the JPEG data.

Here, the restart marker is the control code that resets DPCM used for the compression of DC component of JPEG to the initial value, for the purpose of reducing possibility of propagating code errors. The restart marker is embedded in the compressed data at periodic intervals of a set number of MCU's (Macro Cell Units), there being 8 restart symbols from FFDO to FFD7, with the exception of embedding FFD9 in the case of the last image. The set number of MCU's between restart markers is determined according to the size of the original image.

This paper proposes techniques of overcoming the problems associated with the combination of the compressed data by using the re-start marker characteristics.

The prerequisite is that the recording format is DCF 98. This means that the periodic interval at which restart marker are placed is fixed at 4MCU. Consequently, the input image is made into units of 32 MCU, making the last restart marker of the compressed image always FFD7.

In addition, in order to solve the problem of the variable length of the JPEG data making it difficult to identify the last position of the data when combining the compressed data, a code-counter is built in the JPEG compressor to measure the length of the compressed data.

With the introduction of these techniques, the combination of the compressed data is accomplished by the following 2 steps:

1. After compression, the position of the last re-start marker (FFD9) of the compressed data to be combined is identified by the use of the information obtained by the code-counter.
2. FFD7 is overwritten on FFD9, and it is combined with the next compressed data.

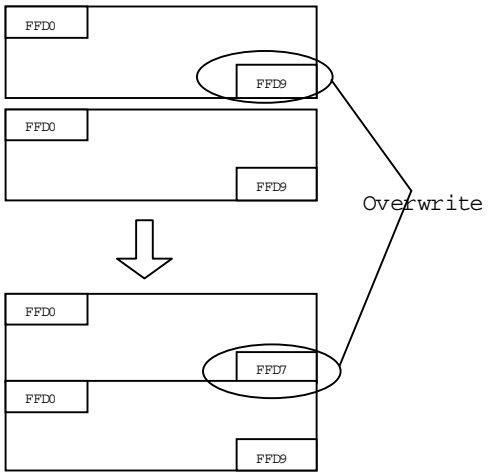

Figure 4. Combination of JPEG-compressed data

3. Prototype System

A prototype semi-folder camera was prepared in order to confirm the effects of our proposal, as shown in Fig. 5.

The prototype system is based on our GX-680III camera, with a unit composed of a CCD and a parallel signal processing circuit replacing the film-pack. Fig. 5 is a complete view of the prototype system.

Figure 5. Prototype system

The system is composed of a single CCD as the image-capturing element, 13 PE (processing elements) as the parallel processing engine, and 1.8-inch hard disk as the recording medium. An LCD is also installed for the recorded-image confirmation.

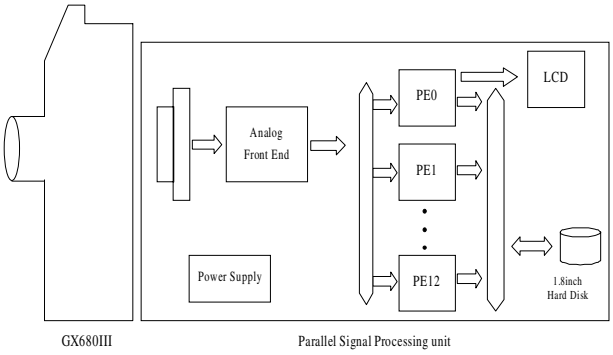

Figure 6. a block diagram of the system.

3.1 CCD

Figure 7. CCD

System name	HA-CCD
Color-filters	G; orthogonal lattice, R & B; mosaic
Effective pixel-numbers	5408(H) x 3824(V)
Chip size	38.83mm x 54.03mm

The employed CCD is a 20M pixel prototype product (5408(H) x 3824 (v) HA-CCD)

3.2 PE (Processing Element)

Figure 8 is a block diagram of a PE. The PE (Processing Element) is composed of a CPU, a signal processing unit, and a JPEG-engine combined into one unit. The PE's are structured into a control relationship composed of PE-0 as the master and the others as the slaves. During signal processing, the master dispatches commands to each slave through the 1 to 1 serial communication channel installed between the master and each slave, and the processing is executed.

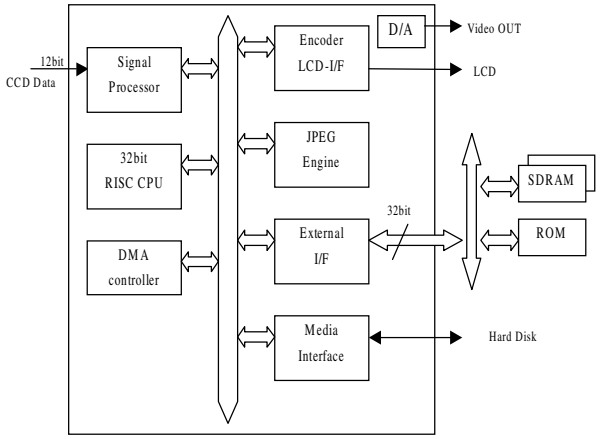

Figure 8. PE (processing element)

3.3 Operation

The control system is composed of the master-slave system. PE-0 plays the role of the master, and others slaves. The processing flow is shown in Fig. 9.

After the CCD data of [a multiple number of 32] MCU's is captured with the overlapping processed parts, the signal is processed and compressed in conformity with JPEG standards. The compressed data is stored in the SDRAM.

After the completion of JPEG compression, the compressed data are combined. Fig. 10 shows the flow of the process combining the compressed data.

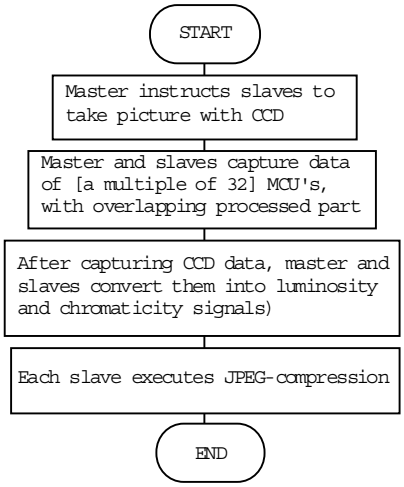

Figure 9. Signal and JPEG processing flow

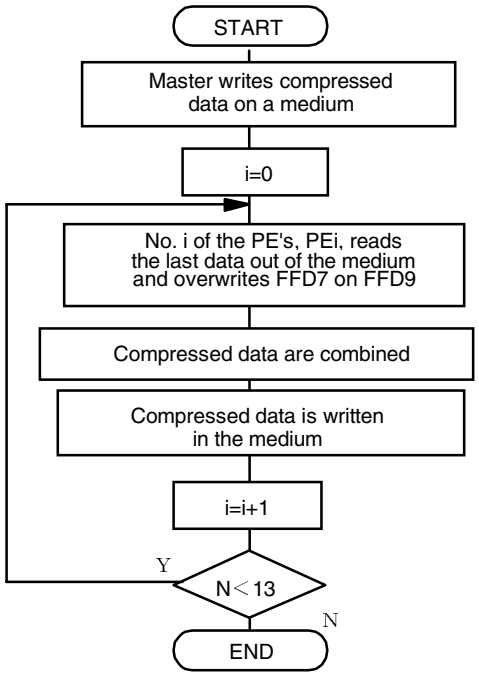

Figure 10. Combination of compressed data

At first the compressed data of the master is recorded in the medium. Slave-1 reads out the last part of the recorded data, overwrites FFD7 on FFD9, connects it with the compressed data that the slave possesses, and writes it on the medium. This operation is repeated for each of the slaves.

During the combination of the compressed data, it is first written on the medium. This action has the advantage of making it possible for a system without an added special circuit for the combination of the compressed data to construct the image, simply by parallel connection of the signal processing systems with the least necessary alteration.

4. Experimental Results

Figure 11 shows the relation between the number of PE's and the processing time.This figure confirms the effect of the parallel processing. The processing time is 4 seconds when there is only one PE, and 1.2 seconds when the number of PE's ≥ 5. Saturation of the rate at PE ≥ 5 reflects the fact that the more the PE in number, the more the traffic needed between the master and the slaves, since the communication is conducted as 1 to 1 serial communication between the master and each slave. Thus the traffic among PE's reaches a level overshadowing the signal processing itself.

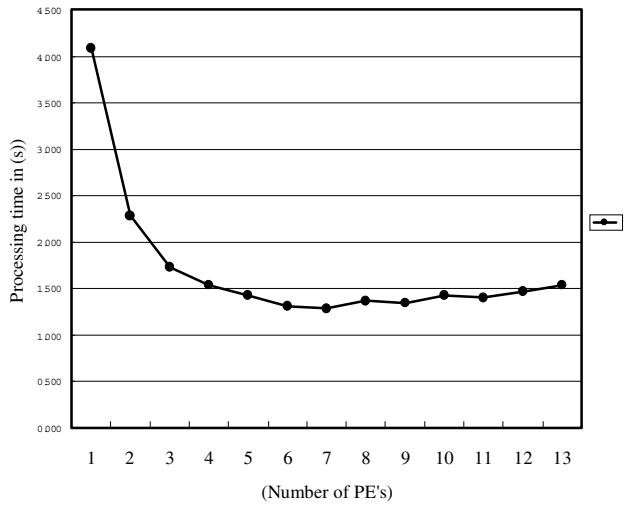

Figure 11 Relation between processing time and extent of parallel processing(without write operation of Hard Disk)

5. Conclusion

This paper described a technique of parallel siganal processing for the digital cameras. The parallel processing was conducted with respect to generation of luminosity and chromaticity signals as well as JPEG processing.

The effect of the proposed technique was confirmed with a prototype product, and it showed that signal processing of 40 M pixels was completed in 1.2 seconds.

Further improvement of this technique is to be attempted, so that the ratio between the extent of the parallel processing and the processing rate is proportional over a wide range, accomplishing this by reducing the traffic among PE's.

References

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Biography

Kaoru Adachi was born in Tokyo, Japan, February 14, 1964. He recieved the B.S. degree in electrical engineering from the Waseda University, Japan, 1986

In 1986, he joined engineering & designing div., electric imaging products div. of FUJI PHOTO FILM CO., LTD, Tokyo, Japan. He is now working on the circuit design of high-speed signal processing of a Digital Camera.