Signal Processing System for High-Resolution Digital Camera

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Abstract

This Paper presents a signal processing system for newly developed digital camera, MX-700 [1)4)], MX-500, MX-600 ZOOM and DX-10. This system comprises a signal processing LSI and multi processing CPUs. The system can realize not only an inexpensive camera for consumer users but also a high performance camera for professional users. It can be changed the system configuration flexibly in accordance with the specification of the camera.

The digital signal processor includes AE/AF function, high-resolution signal processing, peripherals for the RISC processor, digital encoder, D/A converter and SmartMedia controller. The LSI achieves compact, low power and high-resolution image acquisition system. The RISC processor includes an internal DRAM and achieves high-speed operation.

The outlines and main features of the signal processing system are described.

Introduction

The digital camera has shown rapid and widespread market growth as an image input device. Originally, digital cameras with VGA pixel size were the main products on the market, while those with resolution over 1.0 Mega pixels were limited to so-called professional uses: for instance, in the mass press, printing, and other sectors.[2)3)] Recently, there has been an acceleration of the penetration and spread of high-resolution digital cameras within the consumer market.

This time, we have developed some digital cameras by using this system. This system mainly comprises a newly developed signal processing LSI and one some RISC-CPUs with DRAM. The signal processing LSI- with a CCD signal processing circuit, a CPU peripheral circuit, and a SmartMedia interface circuit, etc.-is contained in a CSP (Chip Size Package) so as to realize a compact, high-resolution, and low power-consumption camera.

This paper introduces the configuration of this system, as well as how the camera's function have been realized. This paper also includes a brief description of the storage format for SmartMedia, which is the storage media employed.

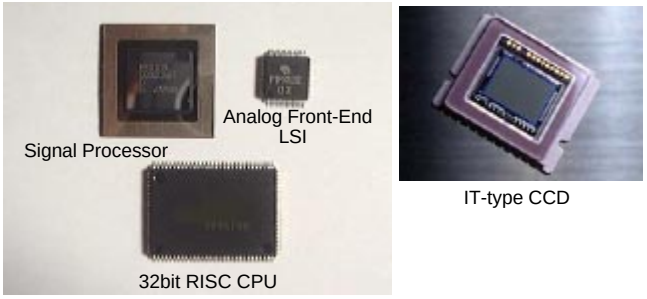

Figure 1. LSIs for this camera system

MX-600 ZOOM System Configuration

The system configuration of the MX-600 ZOOM is shown in Fig. 2. The MX-600 ZOOM comprises an IT (interline)-type 1.5 M pixel CCD [5)], a newly developed analog-front-end LSI, a signal-processing LSI which includes a CPU peripheral circuit, and two sets of RISC-CPUs with DRAM. Fig. 1 shows photographs of the external appearance of the chips. We have employed a 1.5 M pixel IT-type CCD with a color filter of a G vertical-stripe R/B checkered pattern. The analog-front-end IC includes a new pre-amplifier, which enables a higher S/N ratio than the conventional CDS (correlated double sampling)-type and other common pre-amps. The MX-600 ZOOM also incorporates an 18-mm square, 264-pin CSP (chip size package) for signal processing, and a 14 mm x 20 mm 100-pin QFP for the RISC-CPU with DRAM. Owing to its low-power design, 80/250 (LCD on/off) shots can be taken with the MX-600 ZOOM. And even though a 1.5 M pixel system has been employed, lower power

consumption than with the conventional system has been realized for the MX-600 ZOOM.

MX-500 System Configuration

The system configuration of the MX-500 is shown in Fig. 3. The MX-500 is comprised a signal processing LSI and a RISC-CPU. It is achieved lower consumption compared with MX-600 ZOOM by this system with balance processing time and cost. As result, it is realized four AA alkaline batteries as power source. It can take approximately 200 shots when LCD monitor on and 500 shots when LCD monitor off. And, in spite of reducing a RISC-CPU, almost features embedded on MX-700 have been achieved.

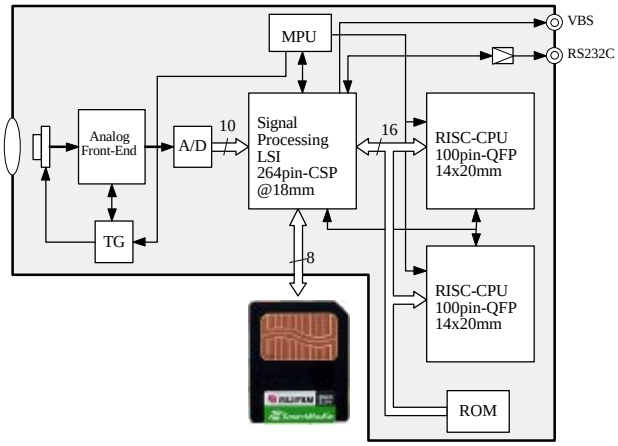

Figure 2. A Block Diagram for MX-600 ZOOM

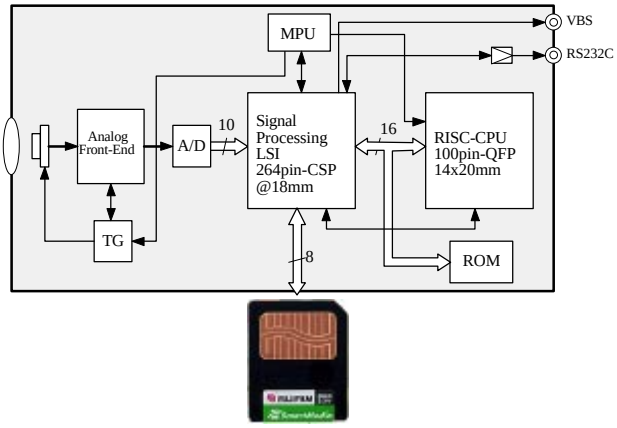

Figure 3. A Block Diagram For MX-500

Signal Processing LSI

Fig. 4 shows an internal block diagram of the signal processing LSI. Each internal block is optionally connected with the 16 bit internal bus. The internal blocks include, besides a signal processor, an interrupt controller as the CPU peripheral circuit, a DMA controller, a timer, a calendar, an A/D, etc. Further, an encoder and a media interface, etc., have also been incorporated.

The signal processor generates luminance/chrominance signals through a G vertical-stripe R/B checkered pattern color filter array by using new algorithm which speeds up processing and delivers sharp, detailed image.

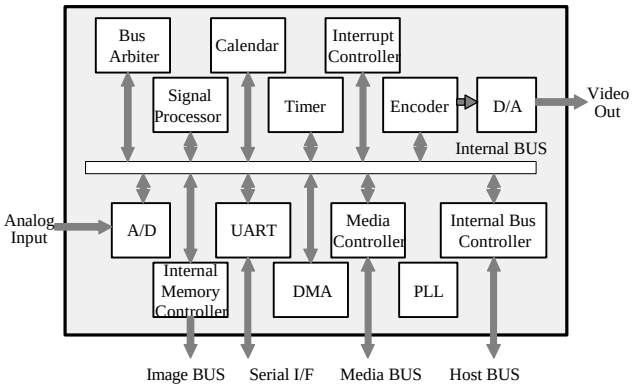

Figure 4. A Signal Processing LSI

Explanation of Camera Operations

In this system, basic camera operations like record/playback are realized mainly with the newly developed signal processing LSI and the RISC-CPU.

In the "movie" operation, the TG(Timing Generator) drives the CCD, and CCD signals are transferred via the analog-front-end LSI, and converted into digital data by the A/D converter for input to the signal processing LSI. The CCD data is buffered in the signal processing LSI, and then transferred to the DRAM in the RISC-CPU for storage by the DMA. At the same time, in the "playback" operation, image data recorded on the DRAM is read out and played back by synchronizing this data with the image synchronous signal for playback. When data for one frame is stored on the DRAM, the playback screen is switched to a different playback screen; by repeating this operation, motion pictures are achieved.

In the "recording" operation, CCD data is converted by the A/D converter; this converted data is stored in the DRAM by DMA via the host bus. Image data for one frame is stored temporarily in the DRAM, and converted into luminance/chrominance signals during signal processing. The luminance/chrominance signals undergo JPEG compression by the RISC-CPU through the use of software; these signals are then stored within SmartMedia, in a

storage format conforming to Exif ver. 2.0. The interval between capturing an image and storing it in SmartMedia has been made as short as roughly 5 sec (without flash). Further, for realization of a fixed length-which is a unique operation of a camera performed to guarantee the shot number-a new bit rate control algorithm has been adopted to realize the target file size for guaranteeing the shot number. To balance quality, processing time and storage requirements, quality mode can be selected.

In the "playback" operation, the image data stored in SmartMedia is expanded while being read out, so as to reproduce the luminance/chrominance signals within the memory. This signals undergo JPEG decompression by RISC-CPU through the use of software. When this expansion has been entirely completed, the RISC-CPU luminance/chrominance signals are transferred to the signal processing LSI to play back the image.

Besides basic camera functions, such additional functions as multi-frame, sepia-color processing, magnification and reduction, digital zooming, etc., can also be achieved with this LSI set. Actually, the camera using this system successfully realizes diversified additional functions by use of the functions just noted.

SmartMedia

SmartMedia has been adopted as the storage medium. The merits of SmartMedia lie in the fact that the medium itself is thin and small-sized; this enables a more compact size for the overall unit. Also a relatively inexpensive price has been achieved because there is no controller, etc., incorporated within the medium. Considering these merits, SmartMedia may be regarded as the most suitable medium for the consumer market.

As for connection with a PC, by using the floppy disk adapter "Flashpath" (the FD-A1; Fig. 5), data on the camera can be transferred to a PC as easily as with a conventional 3.5 inch floppy disk. PCMCIA interfacing is enabled through the use of the PC-AD3, a PC card adapter. And, of course, data exchanges are also possible with any notebook-PC having a PCMCIA slot.

This system is adaptable to both 3.3 volt and 5 volt SmartMedia. Further, based on considerations of future market expansion, a memory capacity of up to 128MB is possible.

The storage format is based on Exif ver.2.0, which is being studied as a possible standard format for digital cameras. Compared with Exif ver.1.1- which has already been adopted as the ISO Standard- Exif ver.2.0 has been improved in several points, including the fact that conversion into FlashPix has been made easier.

Specifically, in Exif ver.2.0, the following points have been added or improved from Exif ver.1.1.

(1) Inclusion of a restart marker
(2) Addition of required tags (color-space tag and FlashPix-ready tag).
(3) APP2 expanded data storage.
(4) Adaptable to arbitrary storage order of JPEG headers.
(5) Adaptable to an arbitary color space.
(6) Playback possible for both 4:2:2 and 4:2:0.
(7) Compressed thumbnails.
(8) Adaptable to voice files (WAVE-format).

In this way, while keeping its previous close relationship with the PC, Exif ver.2.0 has been contrived to newly include camera-unique information.

Conclusion

We have developed some digital cameras that incorporate a newly-developed system that employs a newly developed signal processing LSI and RISC-CPU with an internal DRAM. In this way, our products realizes high-image quality and low-power consumption along with its compact size. And we put on sale some products for wide range market which is from low-end use to advanced use. Then this compact size has been successfully achieved while incorporating the high-resolution CCD, which also enables high picture quality. These features have earned the our products high praises in the digital camera market.

Figure 5. PC Interface (FD-A1/PC-AD3)

References

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