A High Image Quality Fully Integrated CMOS Image Sensor

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Abstract

We describe the feature set and noise characteristics of a production quality photodiode-based CMOS active pixel image sensor IC fabricated in Hewlett Packard's standard 0.5 micron and 3.3V mixed-signal process. It features an integrated timing controller, voltage reference generators, programmable gain amplifiers and 10-bit analog-to-digital converters. It offers excellent blooming-resistant image quality and dissipates 125mW (nominal) for a VGA(640X480) resolution image at 15 frames/sec. Integrated features that simplify overall system design include random access and windowing capabilities, subsampling modes, still image capabilities and separate gain control for red, green and blue pixels. HP's unique CMOS process features a low dark current of 100pA/cm^2. We also describe the low fixed-pattern and temporal noise characteristics of the image sensor.

Introduction

Until recently, digital image capture has been dominated by the charge-coupled device (CCD) which relies upon highly specialized silicon processing that is optimized for the conversion of incident photons into charge but is not suited for further processing of the detected signal. Thus, while CCDs have enabled both efficient and low noise image capture, they require significant support electronics external to the sensor along with the associated engineering effort and PC board space for a complete imaging solution. The promise of CMOS is to provide an integrated imaging solution that is small, inexpensive, draws very low power, and is extremely easy to apply. However, due to the utilization of mainstream, high volume CMOS processes that have not been optimized specifically for imaging, and due to the fact that the practical application of CMOS to image sensing is relatively new, typical CMOS imagers provide inferior image quality than can be obtained from the more mature CCD based technology. The development trend for CMOS imager chips is very steep however. Each new generation of chip design offers higher levels of functionality integrated onto a single chip such that the primary promise of CMOS technology is rapidly being realized. In addition, the combination of improved analog processing techniques and silicon process refinements are resulting in steady improvements in captured image quality.

In this paper we present the design of HP's first standard product CMOS image sensor. The design, having a pixel count of 664X504, is targeted for both video and still image capture applications. In this first offering, the primary design emphasis was on delivering the highest possible image quality while simultaneously providing a flexible feature set for ease of use. The first section describes the chip architecture with particular emphasis on the analog signal path. The second section describes the details of the pixel operation, design and performance. The third section describes operating modes. The fourth section describes parameters important to image quality and provides corresponding measurement results. The fifth section describes the integrated feature set. Conclusions are presented in the final section.

Chip Description

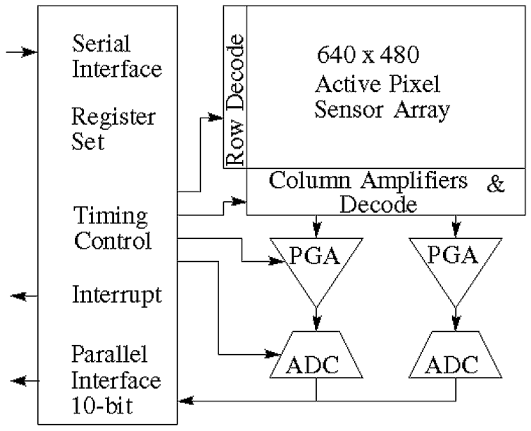

Figure 1. Imager block diagram

A block diagram of the CMOS sensor IC is shown in Figure 1. Approximately 50% of the die area is dedicated to the image sensor with the remainder split between the analog and digital electronics and the pad ring. A dual analog signal path was employed to enable faster readout of the array. The analog path progresses from the pixel outputs to the column amplifiers where an entire row of pixels is simultaneously sampled. The column amplifiers, when selected, provide a differential signal to the programmable gain amplifiers (PGA) which is equal to the difference between the corresponding pixel integrated and reset levels. The PGAs offer an 8-bit programmable gain range from 1 to 40 to match the pixel signal level to the analog to digital converter (ADC) input range and

thus minimize the effect of quantization noise. A successive approximation architecture was chosen for the ADCs because it yields a low power converter with high resolution and does not require calibration. The ADCs achieve approximately 9.4 effective bits of resolution at peak data rate.

One major advantage of integrating the analog electronics on the same chip as the sensor is that the sensitive analog signal does not leave the well controlled environment of the IC. The pixel outputs are immediately converted to a differential form in the column amplifiers by a proprietary sampling technique that gives high rejection of substrate and supply noise while subtracting off the column amplifier offset. The signals are processed in differential fashion by the PGAs and ADCs as well and are thus immune to corruption from common mode noise sources. Offset cancellation is also employed in the PGAs, and a proprietary shared digital-to-analog converter (DAC) architecture is employed between the two ADCs to minimize channel related fixed pattern noise.

Pixel Description

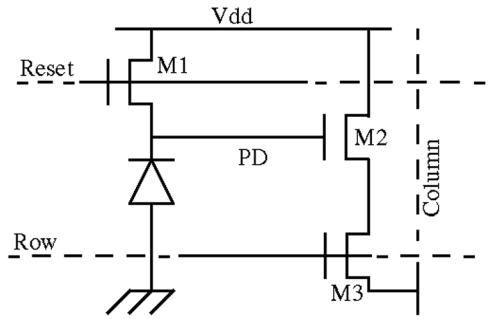

Figure 2. Pixel schematic

The pixel used is a 9µm by 9µm three transistor (3T) design. As shown in Figure 2, the pixel contains 3 NMOS transistors and a photodiode. Transistor M1 resets the photodiode to Vdd-V_{tn} to begin the integration period, and after the end of integration to provide a reset sample. When the row line is asserted, M3 enables the source-follower device M2 to buffer the PD voltage onto the column line. An amplifier at the bottom of each column samples the column line at the end of each integration period, and then again immediately after the sample reset. The column amplifier outputs a signal equal to $V(PD_{reset})$ - $V(PD_{integrated})$.

The physical design of the pixel has parasitic capacitances to the photodiode from both the reset and row lines. Effort was made to minimize the coupling, but elimination is not possible. A proprietary row and reset timing sequence was developed such that any charge pulled off by a falling edge was compensated for by a corresponding rising edge.

The physical implementation of the photodiode sought to minimize the capacitance on the PD node while maximizing the photodiode size for photon capture. Capacitance minimization is key to achieving high sensitivity. The photodiode is formed by n-type implant over a p-type substrate. The junction characteristics are modified, however, compared to the standard source-drain junction to minimize capacitance and enhance quantum efficiency. Junction optimization was accomplished without the addition of masking steps beyond the standard process. The resultant pixel has a capacitance of ~10fF with a 42% fill factor. A conversion gain of 16µV/e- and sensitivity of (1.1V/(Lux-sec)) at 555nm were achieved. Measured quantum efficiency as a function of wavelength is presented in Figure 3.

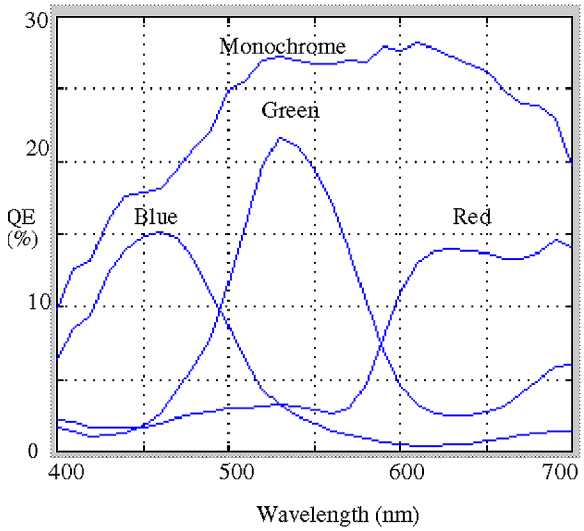

Figure 3. Pixel quantum efficiency without micro lens

The chip was designed in an HP internal mixed signal ASIC process. The foundry was originally optimized for the manufacture of battery powered products, calculators, palmtops, etc., and has inherently low leakage. This resulted in the excellent 100pA/cm^2 dark current performance measured for this pixel.

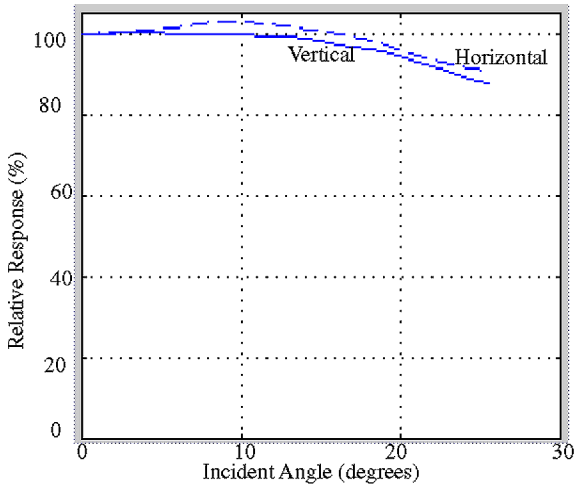

Figure 4. Pixel angular response

The pixel uses RGB pigment based color filters configured in a standard Bayer pattern. These filters are less tem-

perature sensitive than standard die based filters. This allows machine soldering of this component in contrast to the hand solder requirement of many CCDs. Pixel response as a function of incident illumination angle (away from normal) is presented in Figure 4. This plot demonstrates a very wide angle of acceptance resulting in relaxed telecentricity requirements on the optics, possibly allowing for smaller or higher speed optics.[1]

Operating Modes

Rolling Electronic Shutter

For video capture, the most common mode of operation will utilize the rolling electronic shutter. In this mode individual rows are progressively reset to start integration and readout. Figure 5 shows an example setup with an array image window of six rows and an integration time set to 2 row processing times. A row processing period is a programmable value equal to the amount of time required to sample a row of pixels and then digitize the entire row. Each 'Tn' represents a row processing period and each rectangle a row of pixels. In the first period the first row is reset. During T2, the second row is reset while the first integrates. During T3, the third row is reset while rows one and two integrate. In T4, the first row integration is complete, so it is read while the integrate and reset progression steps down and the pattern repeats. In practice, integration times can be set to fractions of row periods such that an exposure granularity of 0.5µsec can be achieved with maximum exposure times extending to several seconds.

Mechanical Shutter Mode

In this mode each row is serially addressed and reset at a minimum timing equal to the reset pulse width plus two clock cycles. After each row in the image window has been reset the shutterSync pin is asserted to open an external mechanical shutter. The shutter remains open until the defined integration period has expired. The array is then readout with the shutter closed.

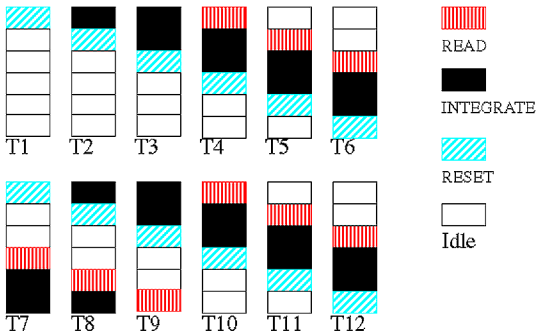

Figure 5. Rolling electronic shutter reset and readout progression

Image Quality

Temporal read noise, fixed pattern noise and the ISO speed of the sensor have a significant impact on the quality of the image captured and that subsequently is displayed or printed. The major factors affecting image quality are discussed next.

Temporal Read Noise

Temporal read noise refers to the random time-dependent fluctuations of signal level due to both fundamental and circuit-oriented noise sources. Photon shot noise is not included in this definition however. The read noise is most problematic when detected signal amplitude is low.

Temporal read noise sources are present in the pixel, column amplifiers, PGAs and the ADCs. The overall temporal read noise (N) can be modeled as

$$N = \sqrt{(N_1 G)^2 + N_2{}^2} \qquad (1)$$

where N_1 is the amplified pre-PGA noise component, N_2 is the un-amplified post-PGA noise component and G is the PGA gain. Pixel reset (kTC) noise is mostly suppressed due to the subthreshold operation of the reset transistor.[2,3] Measurements indicate that *PGA input-referred* rms noise N_1=20 electrons and N_2=56 electrons (PGA gain G=1.0), yielding an overall read noise N=60 electrons. Note that N2 is almost entirely ADC quantization noise. The *PGA input-referred* noise can be further reduced if the minimum PGA gain is set equal to 2.0. This is the optimum setting for minimum PGA gain as the linear range of pixel output voltage then matches the ADC input voltage range. The *PGA input-referred* read noise N_2 is reduced to 28 electrons, while the overall noise N is reduced to 34 electrons (a 4.8dB improvement over 60 read noise electrons for G=1.0).

This compares to read noise levels of about 10-15 electrons for CCDs with analog output. The effective *CCD system* read noise can increase substantially if post-CCD noise sources like the correlated double sampling (CDS) amplifier, PGA, ADC and circuit-oriented noises are factored in. A CCD with comparable conversion gain and ADC LSB size would yield a read noise level comparable to our CMOS image sensor.

The linear full-well capacity of the CMOS sensor is about 62,500 electrons and the corresponding optimized dynamic range (PGA gain G_{min}=2.0) is 65.3dB. High dynamic range images can thus be captured accurately by this sensor. The photon-shot noise limited SNR at linear full well capacity is about 48dB. The large linear well capacity and corresponding high photon shot noise limited SNR result in excellent image and print quality.

We have not factored dark current shot noise in the discussion above. The dark current defined over the entire pixel is 100pA/cm^2. Dark current shot noise can be estimated from the mean dark signal as follows:

$$N_d = \sqrt{\frac{S_d}{g}} \qquad (2)$$

where N_d is the rms dark current shot noise(electrons), S_d is the dark signal (DN units) and g is the pixel conversion gain (DN/electron). The estimated dark current shot noise for an exposure time of 30ms is about 4.3 electrons, and its impact on the overall read noise (N=34 electrons) is negligible.

Fixed Pattern Noise

FPN refers to a non-temporal spatial noise and is due to device mismatches in the pixels & color filters, variations in column amplifiers, and mismatches between multiple PGAs and ADCs. FPN can be both coherent or non-coherent. Row-wise coherent *FPN-like* noise can also result from poor common-mode rejection. This form of coherent noise varies from frame to frame however.

Non-coherent area-wise FPN has been measured to be less than 1%, while coherent column-wise FPN is about 0.5%. Coherent row-wise FPN appears as an offset error, rather than a gain error, and has been measured to be <0.2LSB and detectable only with very high PGA gain settings and a non-saturated sensor digital output.

The low FPN specifications of the sensor makes dark frame subtraction unnecessary and simplifies the image capture process.

ISO Speed

ISO speed of the CMOS sensor was estimated from the exposure level required to achieve a given SNR in the image. The light source was assumed to be clear sunlight with a black body radiation temperature of 5500K. Read noise, photon shot noise and FPN are included in the SNR definition.

ISO speed is defined by the exposure level (E_m) as follows:

$$ISO\ Speed = \frac{10}{E_m} \tag{3}$$

where E_m is measured in Lux-sec.[4] The requisite exposure time (τ) in seconds is given by

$$\tau = \frac{1}{ISO\ Speed} \tag{4}$$

Fig. 6 shows the relationship between ISO speed and SNR for the monochrome CMOS sensor as a function of PGA gain settings of G=1,2,5,10.

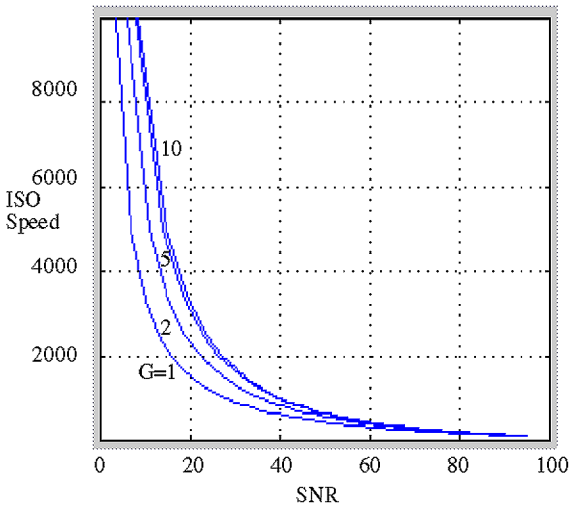

Figure 6. CMOS image sensor ISO speed vs. SNR

The ISO speed is about 3500 for SNR=10 (*acceptable* print image quality[5]) and about 600 for SNR=40 (*excellent* print image quality) when PGA gain G=1.0. The SNR is eventually limited by photon shot noise as the PGA gain increases due to the relative suppression of ADC quantization noise(Fig. 6), and the corresponding photon shot noise limited ISO speeds are 8000 and 1000 respectively.

The high ISO speeds are primarily the result of the large pixel size used (9μmX9μm), and high quantum efficiency

Bloom Resistance

CMOS image sensors inherently have superior bloom resistance due to the presence of the pixel reset device M1 (Fig. 2). Anti-blooming protection occurs as follows. The gate voltage of the reset device is held at zero volts (OFF state) during exposure. The photodiode voltage (PD) drops below the threshold required to turn-on M1 for bright illumination and/or long exposure times. Typically M1 turns-ON in the sub-threshold mode and holds the photodiode node PD to about a few hundred millivolts below ground. This prevents excessive charge buildup at the photodiode node PD, and eliminates blooming.

Integrated Features / Ease of Use

The individually addressable nature of the CMOS pixel array offers two distinct advantages over CCD imagers. First, it allows a sub-window of any size or location on the array to be read out without the overhead of clocking through pixels outside of the desired window. Second it allows skipping of pixel columns as well as rows (horizontal and vertical subsampling) during readout. These capabilities can provide for higher frame rate view finding and potentially more rapid acquisition of focus and exposure information.

Because the imager includes a custom integrated timing controller, the chip operation is easily altered by programming the register set via the serial interface. The programmable features include the following: window size and location, exposure time, PGA gain settings, data and frame rate, pad speed, interface timing, low power modes, and shutter modes. For the case of a Bayer color filter pattern, different PGA gains can be applied to each color pixel to aid in color balance. The peak achievable frame rate when reading out the full VGA window is approximately 15 frames per second, however, either or both horizontal and vertical subsampling can be enabled to increase the frame rate by approximately a factor of two or four respectively. Once the imager is configured as desired, single or continuous frame capture is initiated by asserting the control register run bit. The chip operates off of a single 3.3V supply and nominally dissipates 125mW of power in video operation.

Conclusion

A flexible feature set combined with robust integration offered by the CMOS imager described enable rapid development of imaging systems with the addition of optics, image processing, system control, and display.

Table 1. Imager Summary

Array Size	504 × 664
Pixel Size	9μm
Fill Factor	42%
Dark Current (@22C ambient)	100pA/cm^2
Peak Quantum Efficiency	
Monochrome:	28%
Color:	21%
Linear Well Capacity	62,500e-
Conversion Gain	16μV/e-
System Noise Floor (G=2)	34e-
Dynamic Range (G=2)	65.3dB
ADC Effective Bits	9.4
Sensitivity (@555nm with color filter)	1.1V/Lux-sec
ISO Speed (monochrome, G=1)	
SNR=10	3500
SNR=40	600
PGA Gain Range (255 steps)	1 to 40
Exposure Setting Range	0.5μsec to >10sec
Peak Frame Rate (VGA window)	15 frame/sec
Power Supply	3.3V
Nominal Power Dissipation	125mW

Image quality in CMOS sensors is achieved through optimization of the following factors:

1. suppression of pixel sampling noise
2. minimal addition of circuit noise to the pixel noise floor
3. rejection of common mode supply and substrate noise
4. offset cancellation in the analog path
5. low quantization noise
6. low dark current
7. high quantum efficiency

The first five of these factors are optimized through circuit design, the latter two are properties of the process which can also be optimized.

High quality digital image capture is no longer the sole domain of CCDs. The combination of a low leakage base CMOS process and careful attention to analog design will yield low temporal and fixed pattern noise.

Acknowledgments

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