# A 1.3 Megapixel CMOS Imager Designed for Digital Still Cameras

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## Abstract

VLSI Vision Ltd. has developed the VV6801 color sensor to address the demands of the high resolution color Digital Stills camera market. With a pixel resolution of 1280x1024 it provides high color fidelity with low color aliasing, which is particularly relevant for stills photography.

Control and readout timing requirements are similar and pinout is backward compatible to the VV6850/5850 800K pixel sensors, giving ease of design into existing VV6850 800K pixel applications. The VV6801 has an identical image array size to the VV6850, allowing for existing optics to be used.

All clocking and sequencing controls are user defined, giving maximum flexibility of use. This gives a range of versatile operating modes which can be implemented, including high quality still image capture, full resolution 'Live Video', and exposure monitoring modes. A choice of Horizontal and Vertical subsampled 'Cine' modes are available for increased frame rate, ideal for viewfinder applications.

This device is suited to digital still capture and applications requiring digitization of the pixel output and post processing of the image in hardware or software. The image quality from both sensors can be enhanced by implementation of external noise cancellation techniques, using external frame and line buffering.

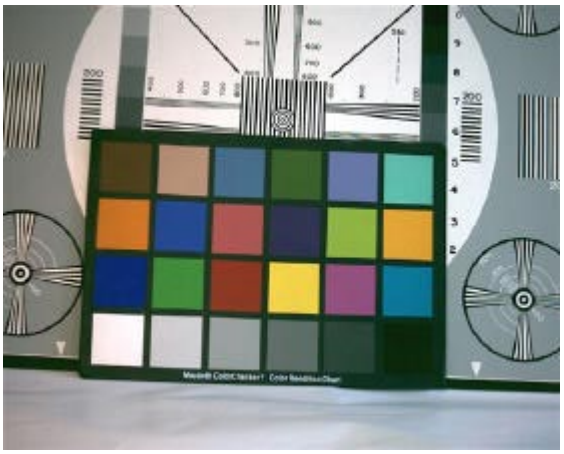
Exposure control can be achieved with or without an electromechanical shutter. The sensor benefits from a pixel fill factor of more than 25%, which has resulted in improved sensitivity. A two way serial interface and control register provides further control and monitoring of certain camera functions.

## Introduction

The VV6801 features a resolution of 1280x1024 pixels, and has been designed as a straightforward upgrade to the VV6850 an 800x1014 element active pixel sensor, APS. While the resolution of the VV6801 is 1.8 times greater than that of the VV6850, advances in pixel architecture, and fabrication processes has allowed the pixel of the 6801 to be shrunk from the 10.8 micron of the VV6850 to 8.4 microns. This means in addition to being a pin for pin replacement for the 6850, both sensors support 1/2-inch format lenses, additionally the 6801 supports microlensing.

The operation of the device takes advantage of other system components found in typical digital still camera, DSC, applications, in order to cancel threshold offsets and dark current FPN inherent to APS arrays that are fabricated on standard digital complimentary metal-oxide semiconductor, CMOS processes. Taking advantage of the frame store feature present in DSCs, for noise subtraction, images of 12-bit accuracy per pixel can be realized.[1]

An additional benefit realized from the CMOS process is the low power consumption of the imager. Voltage input range is from 0 to 5V, and full power consumption is less than 150 mW.



## Sensor Array

### 1.0 Photoplane

The VV6801 image sensor comprises an array of 1306 (vertical, 'lines') by 1028 (horizontal) active photodiode cells feeding into a row of column source followers at the top of the pixel array. These columns are then in turn multiplexed on to four output channels, and finally onto the AVO output. The pixel array is colorized in a four pixel, Red, Green, Blue 'Bayer' arrangement. This provides high color fidelity images with low color aliasing. The pixel array includes a number of reference lines, and a useable image area of 1280 x 1024 'valid video' pixels.

Pixel access is by row and column shift registers. Each row of pixels, or line, is read at the same instant, and stored in a sample-and-hold stage. The columns are then read out alternately, and multiplexed through four output channels to the AVO output stage. The image can then be unshuffled and reconstructed in external buffering and processing circuits. See Figure 1

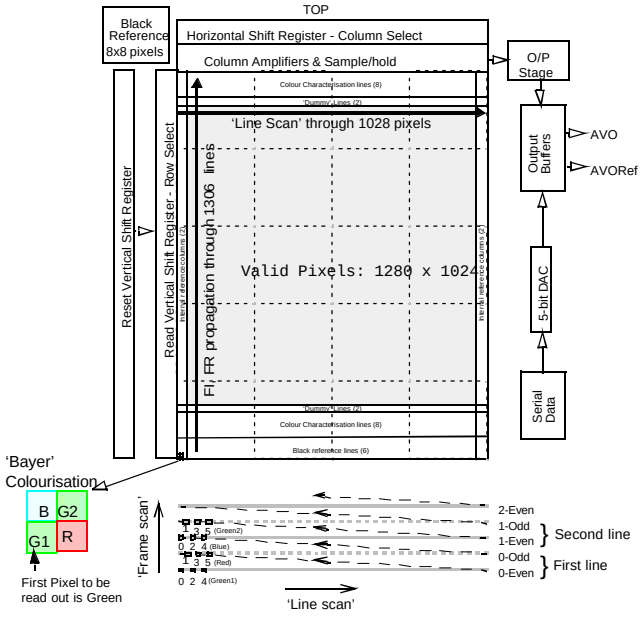



*Figure 1.0 Sensor Array Architecture*

This scheme provides AVO settling to better than 0.1% at a sampling rate of 5 Msps. (Higher sampling rates are possible, with reduced settling accuracy.

Exposure, that is pixel integration time, is controlled by a 'Reset Vertical' shift register with pixel readout controlled by the 'Read Vertical' and 'Horizontal' shift registers. The first ('bottom') 6 lines of the array are black reference lines, followed by 8 color characterization lines, 2 'dummy' lines, 1280 valid video lines, 2 further 'dummy' lines, and then 8 further color characterization lines at the 'top' of the array. The outer two columns on the left and right sides of the pixel array are also internal references, and not read out. Thus the usable image area of the 1306 x 1028 array is 1280 x 1024 pixels. Normal readout (i.e. full resolution 'Live Video' or Still Image capture, Horizontal and Vertical Cine modes not enabled) commences with the even pixels in line 0 (Green1), followed by odd pixels in line 0 (Red), then even pixels in line 1 (Blue), followed by odd pixels in line 1 (Green2).

### 1.1 Vertical Shift Register

The resetting and reading of pixels is performed on a line by line basis, that is a row of column amplifiers reads a whole line of pixel voltages in parallel. The reset/integrate/read cycle for a line of pixels is controlled by the Reset Vertical and Read Vertical shift registers (VSRs).

The length of the 'Frame Integrate' pulse, FI, propagating along the Reset Vertical shift register sets the pixel integration time. FI going high at a point along the VSR releases that line of pixels from RESET, starting the integration period. The two-line 'Frame Read' pulse, FR, which comes at the end of the integration period, starts the field readout, which proceeds from 'bottom' to 'top'. As FR propagates along the Read Vertical shift register, it controls which line is to be read. For exposure control by means of a shutter mechanism, FI should be held high throughout the frame integrate/read cycle.

The Line Clock pulse, LCK, clocks the Vertical Shift Registers. Within a frame, first an even line, then an odd line is read. This is controlled by the EVEN clock, which must be half the LCK frequency and change two PCKs before LS (Line Start) rises.

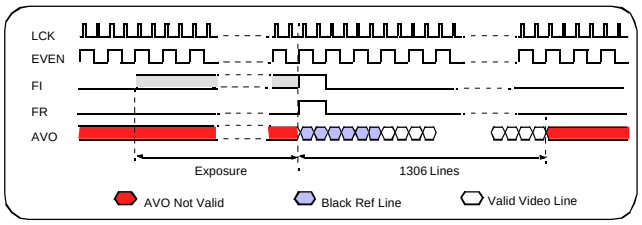



*Figure 1.1 Single Frame Integration & Readout*

### 1.2 Horizontal Shift Register

The Pixel Clock, PCK, clocks the Horizontal Shift Register. Columns are read out, from left to right, by the Line Start pulse, LS, propagating along the Horizontal Shift Register. The LS pulse must be four PCK periods long, with the first valid pixel being sampled after the falling edge. To avoid bandwidth limitations within the output stage causing cross talk problems between the colors in a color pixelated sensor, the horizontal shift register either reads out the odd or the even columns, under control of the EC signal. In order to read valid pixel data, the Pixel Read input to the Read VSR, PXRD, must be pulsed high.

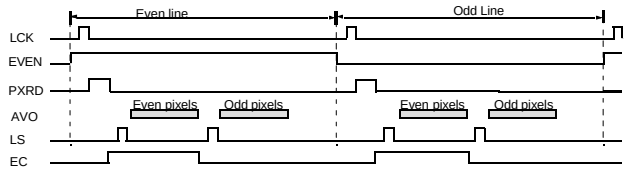



*Figure 1.2 Line Readout Timing*

## Noise Removal

There are many possible ways achieve FPN cancellation in order to produce the highest quality stills images from the VV6801 sensor. The exact method chosen will depend on the intended use of the imager system, and the ancillary devices available in the system, such as the frame buffer and mechanical shutter typical of a Digital Stills Camera. A number of schemes are discussed. In order to obtain high quality, low noise images from the VV6801 sensor pixel the pixel offset variations, or Fixed Pattern Noise (FPN), must be removed. This can be done by reading the image array more than once, for example reading in the dark to establish a reference for each pixel, then reading the exposed array to
collect 'image plus offset' data, then subtracting to remove the offsets. To obtain the lowest noise operation the random pixel 'reset' noise must also be removed.

The major sources of Fixed Pattern Noise in the sensor that can be cancelled are:

- Transistor Threshold Offsets
- Dark Current

Each of the above can be effectively cancelled to a much lower residual random noise level by using the techniques described below. The residual noise sources in the sensor, such as flicker noise, dark current shot noise, thermal noise and ADC Quantization noise, that cannot be cancelled, or are a function of the cancellation techniques, define the overall camera noise performance.

### 2.0 Transistor Threshold Noise Removal

Each pixel amplifier, each column source follower and each output channel multiplexer, has a unique offset caused by process variations in the threshold voltage of the transistors. This offset is independent of exposure, and will be relatively stable with respect to temperature and operating conditions. To remove Transistor Threshold FPN, the VV6801 is used in conjunction with an ADC and either a frame buffer or a line buffer.

#### 2.0.1 Pixel offset removal frame by frame with a shutter:

A frame buffer is used to obtain the pixel to pixel DC offsets for the whole image. Capturing a dark (FPN) frame with the shutter closed, and an 'image' frame with the shutter open obtain the offsets. The 'clean' image data can then be extracted by subtraction. (This technique can only be used with a physical shutter, and with at least one extra dark frame acquisition period.)

#### 2.0.2 Pixel offset removal frame by frame with a reference frame:

A non-volatile frame buffer is used to obtain the pixel to pixel DC offsets for the whole image at camera build. These offsets are then subtracted from the exposed 'image' as it is read to obtain the 'clean' image data. (This technique gives

the fastest frame acquisition time at the expense of accuracy.)

#### 2.0.3 Pixel offset removal line by line:

A line of pixel information is read and stored in a line buffer. The line is then reset to black using the CDSR signal, before being re-read to obtain the pixel to pixel DC offsets for that line. As the line is re-read the offset data for each pixel is subtracted from the value stored in the line buffer, the result being the 'image' data. (The COLsam signal must be used to ensure that samples in the same line have the same integration period.) With line by line offset removal the time for reading out a complete frame is doubled, since each line has to be read twice. It is also not possible to remove pixel reset noise or dark current, thus there is a trade off between the frame readout rate and image quality, and the amount of memory required.
Full frame offset removal can be achieved in many ways, depending on what ancillary devices are available in the camera system, and constraints such as image quality required and acceptable minimum frame readout rate.

### 2.1 Dark Current Removal

The 'dark current' in a pixel photodiode is the inherent leakage that discharges the integrating capacitance in the same way as incident light. Hence, Dark Current FPN builds up on the array whenever the array is released from reset that is when FI is high. This means that the amount of dark signal depends on exposure time, and varies from pixel to pixel.

The same degree of dark current charge build-up occurs in the array whether or not the array is exposed to light. Therefore, if the array is allowed to integrate (FI high) with no incident light for the same length of time as for the image exposure, the dark current element of the exposed image data can be ascertained and removed from the image data by subtraction, leaving behind the dark current shot noise. Since dark current also depends on temperature the dark frame should be taken close in time to the image frame, in order to avoid ambient temperature variations.

### 2.1 'Reset Noise' Cancellation

One random noise source that can be cancelled is 'reset noise' (or 'kTC' noise), which is due to the switching of the photodiode capacitance when the pixel is released from reset. This is present in all subsequent reads of the array (without reset) to the same extent. These can therefore be extracted by reading the array immediately after reset (when FI goes high) and subtracting the value obtained from the 'exposed' array data.
This operation also cancels Pixel Threshold Offsets.
To achieve reset noise cancellation, FR should be taken high for two LCK periods when FI goes high, and 1306 lines read before the array is exposed to the required image. The pixel data from this pass of FR through the VSRs must be stored in a frame buffer, and subtracted from the exposed image data. The exposed image is obtained when FR is pulsed high again, coincident with the last two LCK periods of FI being high after the exposure period.

## Operating Modes

While there are six main operating modes for the sensor, this paper will only discuss implementation of the first two. The six main modes of operation are:
1. Still Image Capture with a Frame Buffer
2. Correlated Double Sampling (line by line FPN cancellation)
3. Live-Video Mode
4. Subsampled Mode (Horizontal and Vertical 'Cine' modes)
5. Parallel Integration
6. Accumulate

### 3.0 Still Image Capture with a Frame Buffer

This is the recommended operational mode for high quality still image capture in camera systems where there is an electro-mechanical shutter in front of the sensor and a Frame Buffer for temporary image storage. FPN cancellation is central to this mode of operation, and is described in detail. Other operational schemes that may be devised can include all or some of the techniques employed in this example, but the elements are essentially the same.

The basic still image capture cycle starts with the shutter closed. The array is released from reset by taking the input to the reset vertical shift registers, FI, high. The system controlling the camera must then wait for 1306 lines to allow this "integrate wavefront" to propagate through the shift register, before opening the shutter. When

FI goes high FR should also be pulsed high for 2 lines to initiate the Read sequence. Reading each pixel as soon as it is released from reset yields a reset image which contains both the fixed pattern noise component for each pixel and the random reset noise due to that particular reset operation. This image should be stored in a frame buffer.

When the shutter has closed after exposure FR must be pulsed high again for 2 lines to re-read the array and obtain the exposed image data. Again, it will take 1306 lines to read all of the array pixels. FI should fall when FR falls, to return the active pixel array into reset. As the image frame is read out the appropriate pixel reset value, as stored in the frame buffer, is subtracted from the current pixel value and the result written to the frame store. This removes both pixel reset noise and pixel to pixel DC offsets from the image.

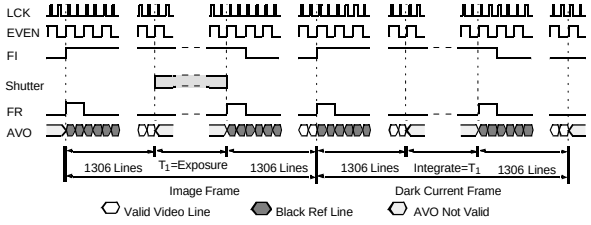



*Figure 3 : Relative timing of still image capture with frame buffer*

Due to the length of time taken to read out an image (200 ms, assuming a 5 MHz clock rate), the dark current in each pixel is a significant part of the image data. To remove the fixed pattern noise injected by the dark current a 'dark image' must be captured with the same integration time as the exposed image but with the shutter closed. Subtracting the dark image from the exposed image removes the dark current fixed pattern noise, leaving a 'clean' image. This process can be summarized as follows:
1. With the shutter closed, release the sensor from reset and immediately read a frame into the buffer memory; this captures the array threshold FPN and reset noise ('V Reset')
2. After 1306 line periods, open the shutter and expose the sensor to the required scene
3. Close the shutter and immediately read the array; as each pixel is read, subtract the value for that position stored in the frame buffer, and overwrite that pixel location with the difference — the memory now contains the image plus dark current FPN (V im + V Dark )
4. After the 1306 line periods of the second read, repeat the image capture cycle, but do not open the shutter; this time, load a second frame buffer with first the V Reset value and then the V Dark value (after subtraction)
5. After the second integration period, subtract the V Dark value for each pixel that is stored in the second frame buffer from the (V im + V Dark ) value for that position stored in the first frame buffer and overwrite that pixel location with the result. The frame buffer now contains the corrected image values, which can be processed for color and so on, then transferred to permanent image storage memory.

Note: Since the 'integrate wavefront' must propagate through the VSR, the point at which the open shutter exposure occurs will vary progressively from line to line of the array — from close to 'Read2' on the bottom line to close to 'Read1' at the top.

### 3.1 Correlated Double Sampling (line by line)

This is an alternative FPN cancellation mode for camera systems where there is only a Line Buffer available for temporary image capture, and not necessarily a mechanical shutter in front of the sensor. The method outlined below, using the CDSR signal, relates to a still image capture in a shuttered camera system, but the same principle could also be applied to exposure control with the FI pulse duration in Still Frame and Live Video modes.

Note: This method does not cancel dark current FPN, and as the pixel is reset twice, has two lots of 'reset' noise sources.

The array is released from reset by taking the input to the reset vertical shift registers, FI, high. The system controlling the camera must then wait for 1306 lines to allow this integrate wavefront" to propagate through the shift register, before opening the shutter (or further extending the FI pulse). After the sensor has been exposed for the appropriate time, FR must be pulsed high for 2 lines to read the pixel array and obtain the exposed image data, which is loaded into the Line Buffer line by line. When a line of 1028 pixels of image data has been read, the CDSR signal is pulsed high to reset the line of pixels to Black (without advancing the HSR). COLSam is then pulsed to resample the row, and as each pixel is read out this 'Black Offset' value is subtracted from the value stored in the line buffer and the result passed on as corrected image data.

Note: During the 1280-line image data readout, LCK and EVEN must be at least twice their minimum periods (with maximum PCK rate of 5.0MHz), to allow for the second line read.

| **Extent of noise cancellation** | **Signal/Noise ratio** |
|---|---|
| No noise cancellation | 26dB |
| Pixel offset fixed pattern noise cancelled | 52dB |
| Pixel offset + Dark current leakage noise cancelled | 58dB(@200mS integration) |
| Pixel offset + Dark current leakage + Pixel reset noise cancelled | 66dB(@200mS integration) |
| **Noise sources which cannot be cancelled:** | |
| Flicker noise<br>Thermal noise<br>ADC Quantisation noise<br>Dark current 'shot' noise | |

*Table 1. Results of Noise Reduction Techniques*

| | |
|---|---|
| Image Format | 1024 x 1280 pixels |
| Pixel Size | 8.4µ x 8.4µm |
| Active Array Size | 8.60mm x 10.75mm |
| Sensitivity (colour) | 50mV/lux @ 50ms exp |
| S/N | Typically 66dB (with FPN cancellation) |
| Max. pixel rate | 10Mpix/s (5Mpix/s for 0.1% settling |
| Power Supply | 5v ±5% |
| Power | < 150 mW |
| Temperature | 0°C - 40°C |
| Package | BGA or 84LCC |

*Table 2.0 Technical Specifications*

*Picture 2. Typical Application*

## Conclusion

As has been shown, the VV6801 has incorporated all the features required by the competitive Digital Still Camera market, high spatial resolution, large signal to noise ratio, standard electronic voltage levels, and very low power consumption to finally realize the promise of CMOS based imagers for effective incorporation into digital still cameras.

[1] J.E.D Hurwitz, An 800K-Pixel Color CMOS Sensor For Consumer Still Cameras, SPIE Photonics East, San Jose CA, 1997