Microelectronic Device Design for a Fully-Integrated Silicon-Based Thermal Ink Jet IC

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Abstract

A thermal-ink-jet printhead which produces high-speed laser-quality printing was introduced by Xerox Corp. in 1993. The thermal power needed to eject the ink drop is generated with a novel IC architecture which consists of on-chip integration of the 128-heater elements, the 5-V addressing logic, the 13-V predriver circuitry, and the 38-V power switches. This integration requires several microelectronics process and device design trade-offs. Because the printhead is a customer-replaceable unit highly-effective electrostatic-discharge-protection devices (ESD) are needed. In this presentation, the specific design issues and failure mechanisms of the high power metal-oxide-semiconductor field-effect transistor switches, and the ESD-protection devices are illustrated through two-dimensional numerical modeling, including parasitic-bipolar and lattice-heating effects, and electrical characteristics of recently fabricated devices.

Heater Wafer Circuit Architecture & Fabrication Trade-offs

The thermal ink jet (TIJ) marking process uses a heater element located in an ink filled capillary tube to create a steam bubble and drive an ink droplet toward the paper[1,2]. A side-shooter ejector, as shown in Figure 1, generates ink drops at a 5 kHz rate (200 μs channel refill speed). If 128 of these ejectors are placed on one printhead, over 3 pages/minute at 300 spots per inch (spi) resolution can be printed, and TIJ productivity approaches that of laser xerographic page printers. Cost-effective and reliable fabrication of 128 drop ejectors is feasible when heater-addressing logic and power switches are integrated on the same chip as the heater elements. This reduces lead count from 1 lead per heater (i.e., *passive* design) to a total of less than ten logic control and power supply lines resulting in a significant reduction of chip size and cost. A schematic of the resulting *logic-on-board* chip architecture is shown in Figure 2. A 32-bit shift register sequentially accesses 4 heaters at once. The data is shifted-in through a 4-bit register, and determines which of the 4 heaters will generate the power to nucleate a bubble. The gate voltage of the power switches is provided by predrivers operating at an on-chip generated 13-V.

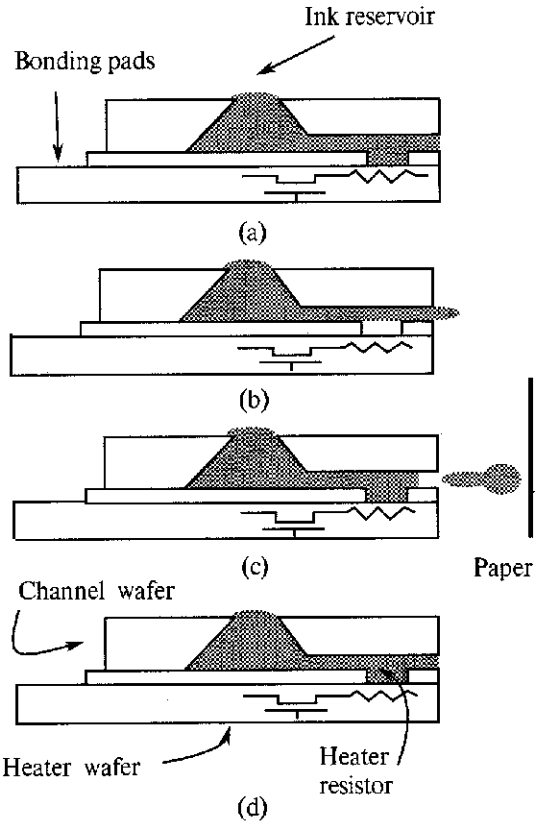

Figure 1. Cross-section of a side-shooter drop ejector during a firing sequence at time steps: (a) 0 s. (b) 3 s. (c) 20 s. (d) 200 s.

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Because the cartridge is a commodity product and it is thrown away once the ink reservoir is empty, the fabrication cost has to be kept to a minimum. The logic part of the chip is not limited by speed, size or power dissipation, a hence a low-cost, high-yielding 5-μm NMOS process flow was chosen as starting IC technology. The process flow was modified to obtain the power switches and the tantalum-coated n^+- polysilicon heater elements. The optimization of themicroelectronic driver and logic transistor parameters affects the heater element operation and vice versa. As an example, the field-oxde used to isolate the logic transistors is also used as the isolation of the heater elements from the substrate. The field-oxde thickness is limited to a minimum of 1.3 μm by the need for heater isolation. The resistor elements are made of the same polysilicon as the gates of the driver and logic transistors. Including aluminum passivation, the resulting merged technology (power switches, heater elements, and low-voltage transistors) can be cost-effectively fabricated with less than ten photolithography steps.

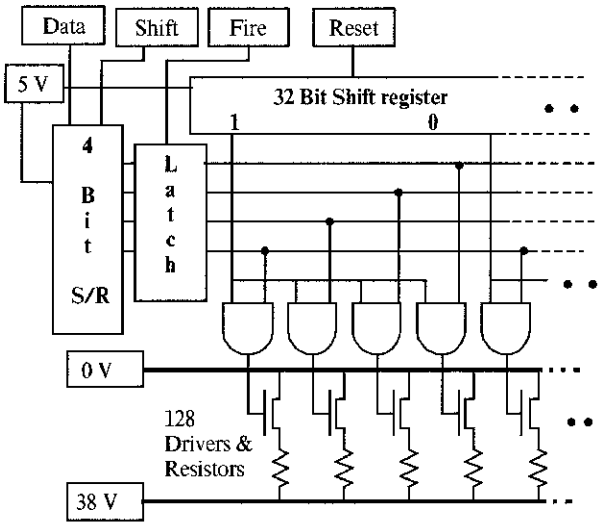

Figure 2. Thermal ink jet logic-on-board chip architecture for a 300 spi. 128 element printhead.

High-Voltage Current Switches

For the vapor bubble to nucleate and the ink droplet to eject at a 300 spi resolution, a 3 μs - 7 Watt pulse must be generated in the heater elements. This requirement places three boundary conditions on the design of the power switch. Firstly, during the short firing pulse the power switches have to supply a high current (200 mA) with a voltage drop across the switch of less than 4 V. This requires the switch on-resistance to be 20 Ohm or below. Secondly, when not firing the switch must be able to withstand voltages in excess of the 38 V supply voltage. Thirdly, the lateral width available to lay-out the switch is set by the printing resolution and for a 300 spi printhead it is limited to 84.5 μm. These requirements can be achieved by using lateral power n-MOSFET switches which can be build within the 5-μm bulk n-MOSFET logic process flow with two additional implant steps (drift region and p^+ substrate contacts). Lateral power MOSFETs with a variety of features were simulated using the process simulator SUPREM3, and the device simulator MEDICI[3]. With the correct model parameters, and after taking lattice heating effects into account, excellent correlation between the simulations and the experimental data is obtained. The simulations accurately predict the breakdown and device on-resistance, and enable the role of the device parameters such as the drift region sheet resistance and the grounded aluminum field plate to be comprehended. Results shown in Figure 3a indicate that when the drift region sheet resistance increases, the breakdown voltage of the driver increases at the expense of increased on-resistance. Adding an aluminum field-plate on the other hand, increases the breakdown voltage without sacrificing the device on-resistance (Figure 3b).

Electrostatic-Discharge Protection Devices

Because the printhead is a user-replaceable unit the IC input pads have to be protected from static discharge to a far greater extend than in state-of-the-art VLSI circuit chips. A thick field-oxide n-MOSFET with the aluminum drain metallization shorted to the Al gate is used as the protection device for the logic input pads. Following ESD structure destruction the wafers were Wright etched to delineate the silicon crystal defects and a circular hole in the drain contact area was observed. This damage results from aluminum alloying through the n^+ diffusion region into the p-type substrate when the eutectic temperature of the Al/Si system (i.e., 577 °C) is reached[4-5]. The ESD human-body-model (HBM) hardness increased from 12 to 16 kV when the distance between the drain junction and the aluminum contact increased from 8 to 20 μm. To clarify this failure mechanism, the ESD MOSFET was modeled using the 2-D simulators SUPREM4 and MEDICI. The simulations results indicate that even though the ESD MOSFET channel inverts before the device breaks down, breakdown is not due to impact ionization of the channel electrons at the drain. It is due to parasitic-bipolar action stimulated by the substrate hole current generated by the avalanche breakdown of the drain-to-substrate junction[6]. At failure a hot spot (with local temperatures in excess of 1000°C) is located underneath the oxide/silicon interface, inside the drain junction. The lattice temperature drops sharply with distance from the hot spot, and failure occurs when the drain metal reaches 577 °C. The simulated DC drain current for which failure occurs increases with increased junction-to-contact spacing, which explains the ESD hardness increase experimentally observed (Figure 4).

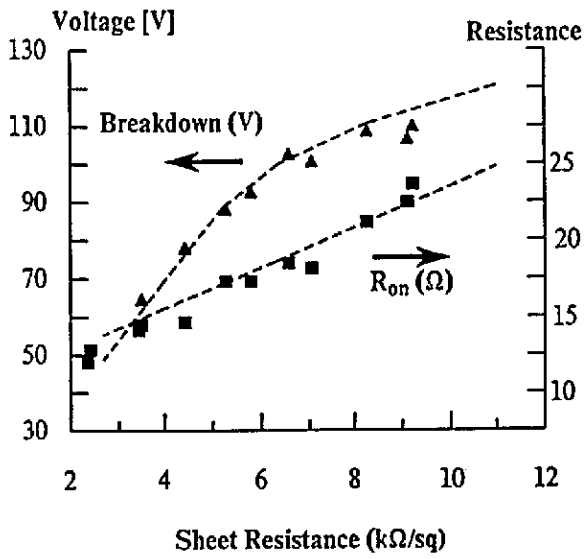

Figure 3a. Driver breakdown voltage and on-resistance dependence on drift sheet resistance. Dotted line are simulation results, symbols are experimental data points.

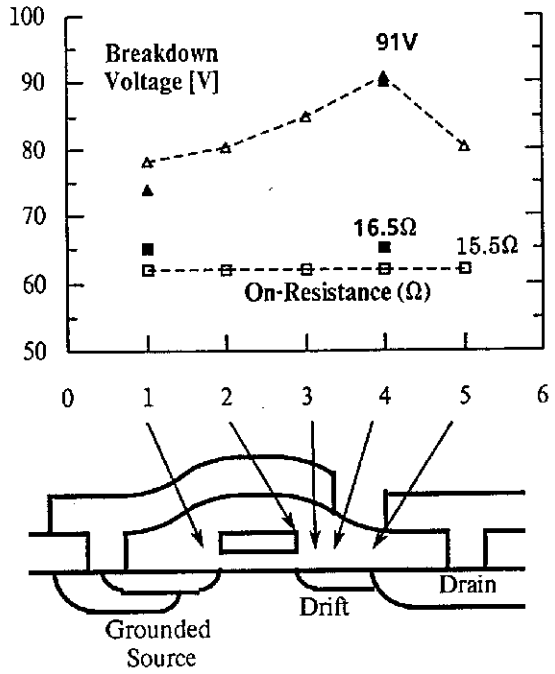

Figure 3b. Driver breakdown voltage and on-resistance dependence on aluminum field plate extention over the drift region. Open symbols and dotted lines are simulation points, closed symbols are experimental data points.

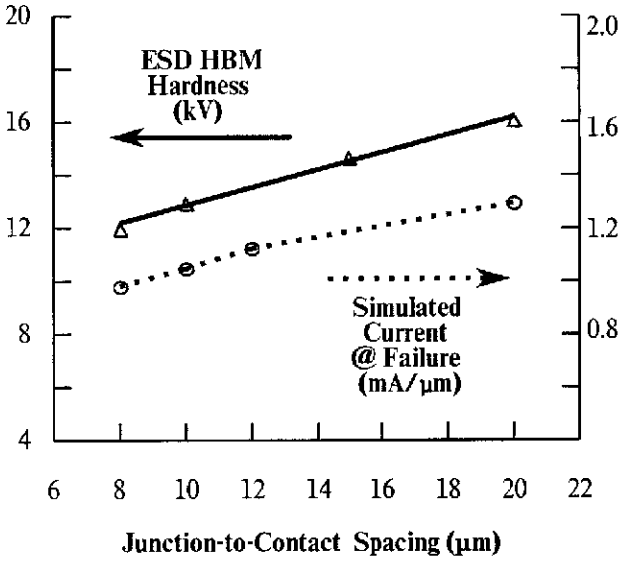

Figure 4. Measured ESD human-body-model hardness and simulated DC current for which Al/Si euteectic temperature is reached at the drain contact.

Summary

A thermal-ink-jet printer with print speed and quality close to that of a laser printer was recently commercialized by Xerox Corporation. The high-speed printing was made feasible through the high level of on-chip drop ejector integration and the novel logic-on-board chip addressing architecture. The resulting advanced TIJ engine was based on a fully-integrated 5-μm silicon nMOSFET technology. The effective heat transfer from the heater element to the ink required the need for several microelectronic chip processing trade-offs. Two-dimensional modeling tools, optimized for power device applications, were used to design efficient and reliable power switches and electrostatic-discharge-protection devices. This novel approach to TIJ printhead design clearly demonstrates the great potential of silicon-based microelectronics to push the limits of thermal ink jet printing speed, quality, reliability and cost.

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